

ZZZ



PCB LA-H351PR10 REV A00 MB  
DAB0004H010  
PCB@

# Coffee Lake-H 45W CNL PCH-H with nVIDIA N18E

REV : 1.0 (XA00)  
2019.04.12



@ : Nopop Component  
EMI@,ESD@,RF@ : EMI/ESD/RF part  
CONN@ : Connector Component  
@EMI@,@ESD@,@RF@ : Total debug Component

Layout Dell logo



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REV: X00  
PWB: XXXXX  
DATE: 1450-06

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NV		PCB Revision
0	0 ohm	EVT-1
1	12k ohm	DVT-1
2	15k ohm	DVT-2
3	20k ohm	Pilot

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Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87

Power Plane	Description	S0	S3	S4 / S5
VIN	Adapter power supply	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1VALW	System +1VALW power rail	ON	ON	ON*
+1V_PRIM	System +1VALW power rail	ON	ON	ON*
+VCCIO	+1.0VS IO power rail	ON	OFF	OFF
+VGA_PCIE	+1.0VS power rail for GPU	ON	OFF	OFF
+MEM_GFX	+1.5VS power rail for GPU	ON	OFF	OFF
+1.2V_VDDQ	DDR-IV +1.2V power rail	ON	ON	OFF
+1VS_VCCST	+1.0V power rail for CPU	ON	ON	OFF
+1VS_VCCSTG	+1.0VS power rail for CPU	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*
+3V_LAN	+3VALW power for LAN power rails	ON	ON	ON*
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VALW	+1.8VALW power rail for PCH	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

Config

LM-431AG631L01:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/17-9300H8/HM370	B8/N18EG08/
LM-431AG631L02:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/17-9750H	MP8/HM370 SSPCE8/N18EG08/
LM-431AG631L03:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/17-9750H	MP8/HM370 SSPCE8/N18EG18/
LM-431AG631L04:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/17-9750H	MP8/HM370 SSPCE8/N18EG18/
LM-431AG631L05:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/17-9850H8/HM370	B8/N18EG28/
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LM-431AG631L08:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/17-9750H	MP8/HM370 SSPCE8/N18EG38/
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LM-431AG631L54:	0478/04708/1288/178/PCHES8/PCB8/PERICOM8/CMC8/LCDTESTEC8/NV8/QX18/U058/UT48/EC8/BID_DVT28/RTD38/19-9880H8/HM370	B8/N18EG38/

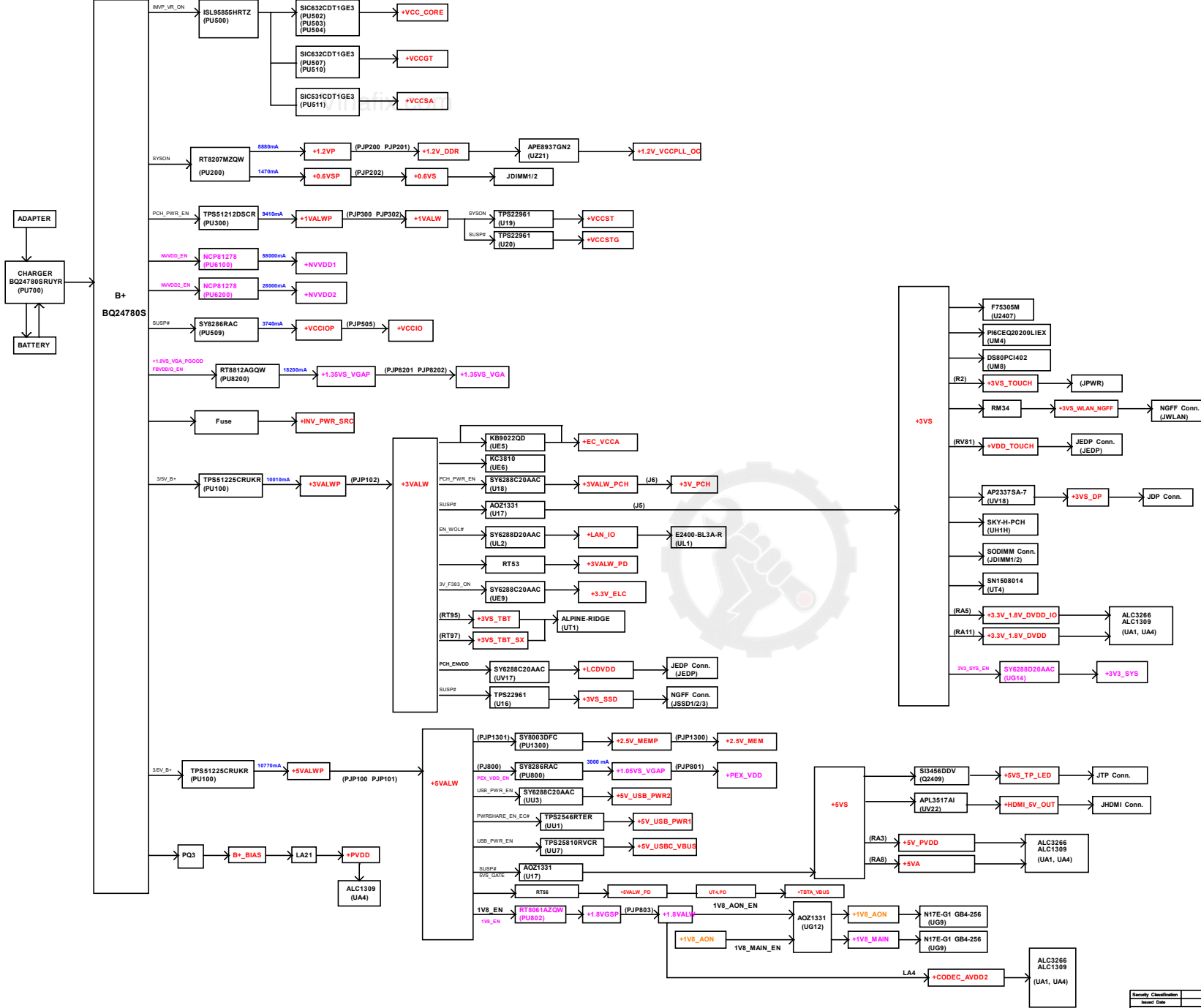
Config-X76 Memory

```
LM-X7681531L10:MCN16G@/DDP16G@/Micron_16G@
LM-X7681531L09:SAM16G@/DDP16G@/Samsung_16G
LM-X7681531L11:HYX16G@/DDP16G@/Hynix_16G@
LM-X7681531L06:SAM8G@/SDP8G@/Samsung_8G@
LM-X7681531L07:MCN8G@/SDP8G@/Micron_8G@
LM-X7681531L08:HYV8G@/SDP8G@/Hynix_8G@
```

Config-X76 Vram

LM-X7681531L02:Vram	Micron@/MCNGD8@
LM-X7681531L01:Vram	Samsung@/SAMGD8@
LM-X7681531L55:Vram	Micron@/MCNGD6@
LM-X7681531L54:Vram	Samsung@/SAMGD6@

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				<b>LA-H351P</b>		
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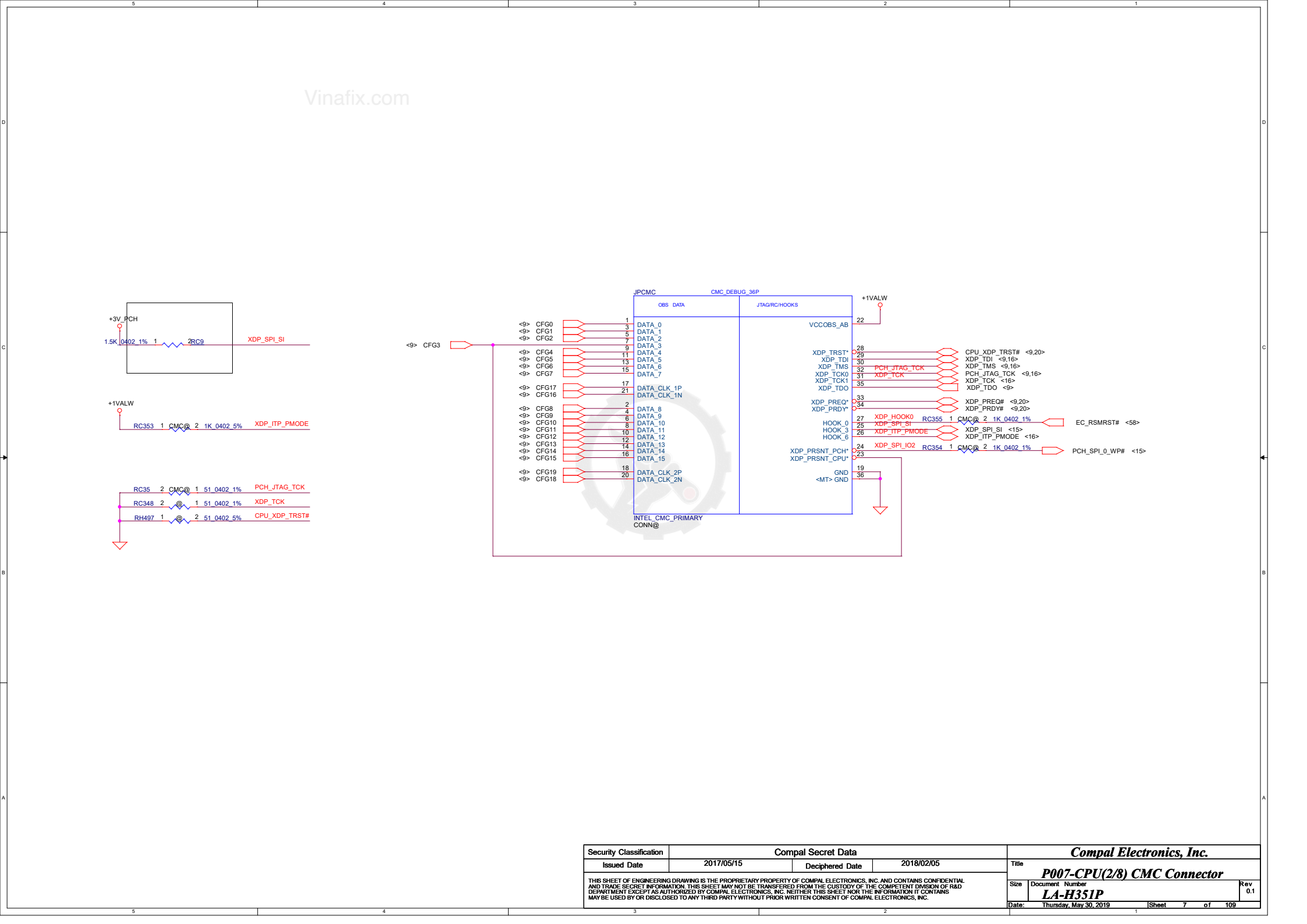


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Date: 2018.05.01					18





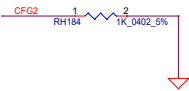




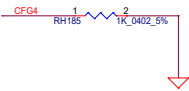
Vinafix.com

Net : DDR\_RCOMP0  
Net : DDR\_RCOMP1  
Net : DDR\_RCOMP2  
Trace Width/Space: 15 mil/ 25 mil  
Max Trace Length: 500 mil

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed



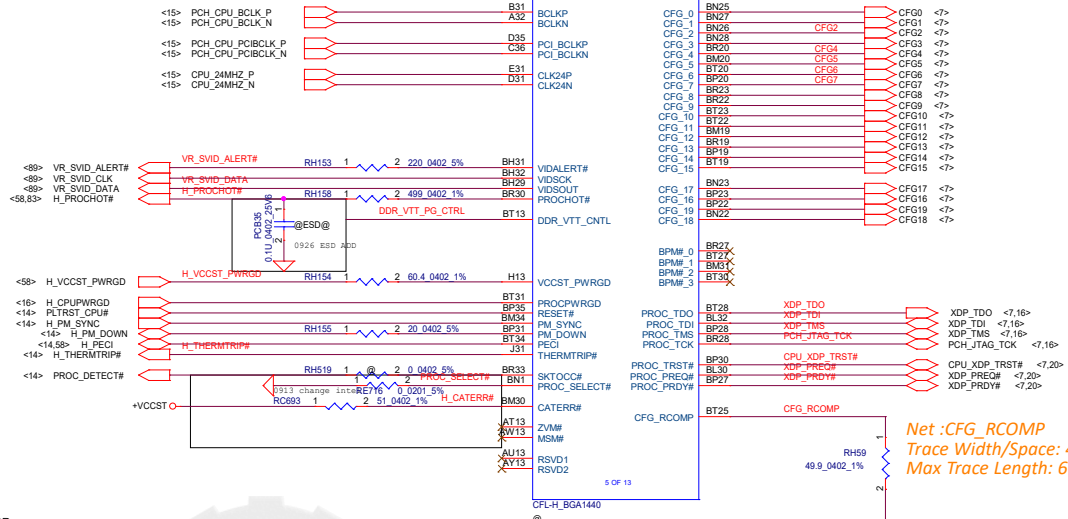
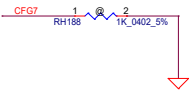
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port ★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



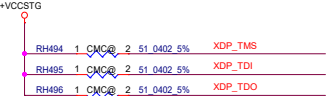
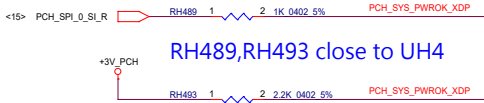
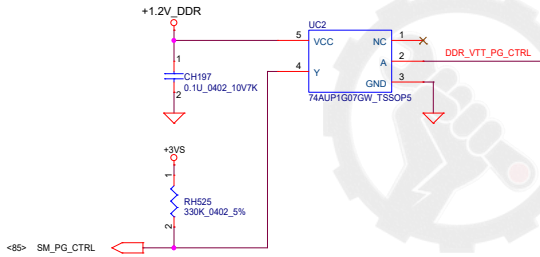
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) ★ 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



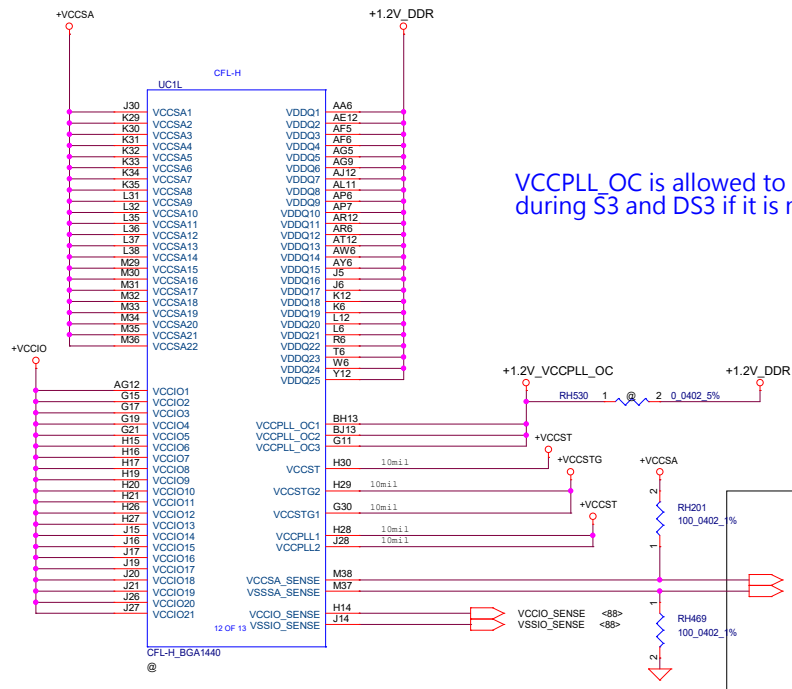
PEG DEFER TRAINING	
CFG7	★ 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



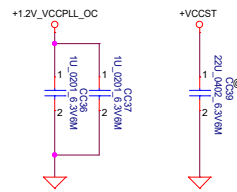
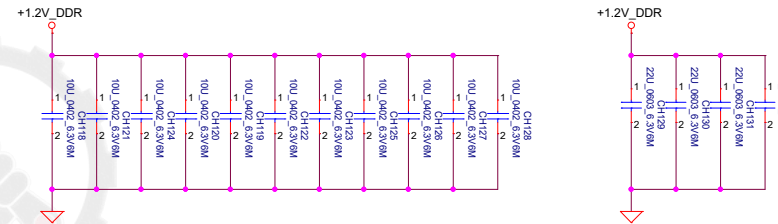
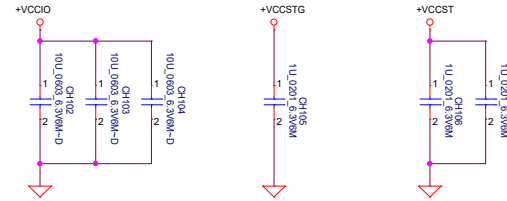
Net :CFG\_RCOMP  
Trace Width/Space: 4 mil/ 12 mil  
Max Trace Length: 600 mil





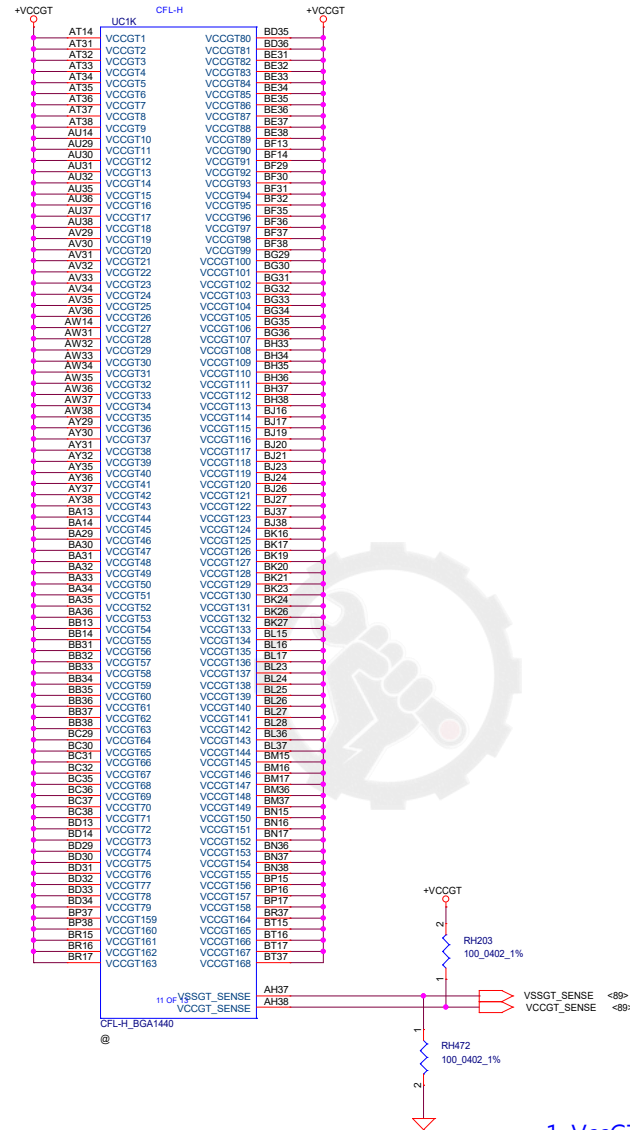


VCCPLL\_OC is allowed to be turned off during S3 and DS3 if it is not powered directly from VDDQ



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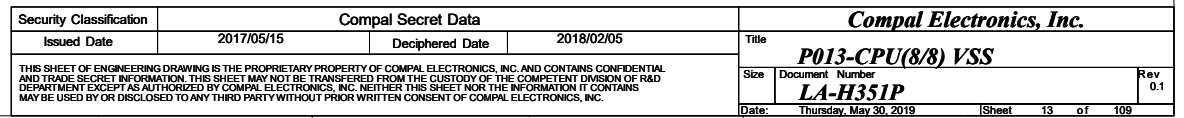
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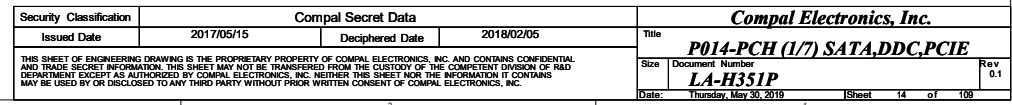


1. VccGT\_SENSE / VssGT\_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1, RC2 should be placed within 2 inches (50.8 mm) of CPU

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Net : XCLK\_BIASREF  
Trace Width/Space: 15mil /15 mil  
Max Trace Length: 1000 mil

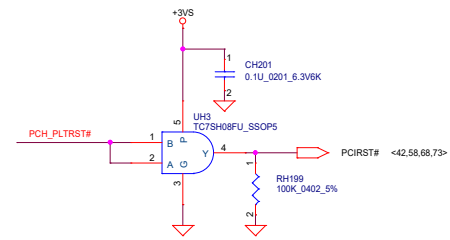
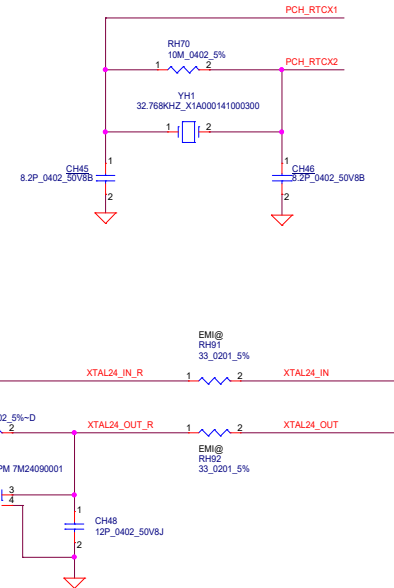
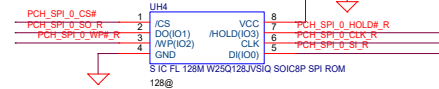
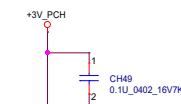
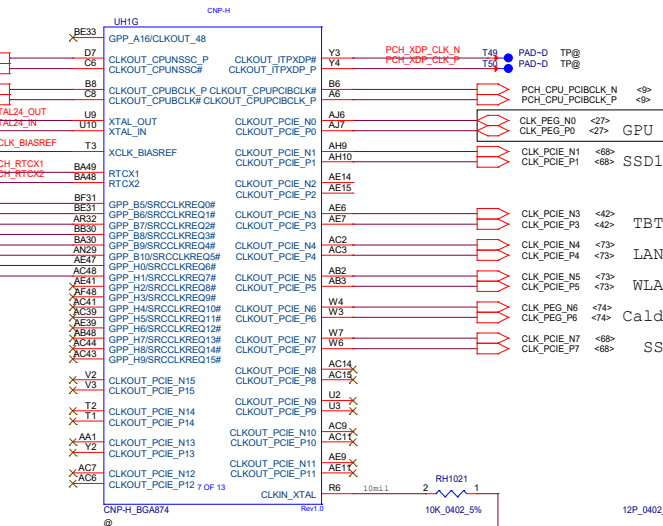
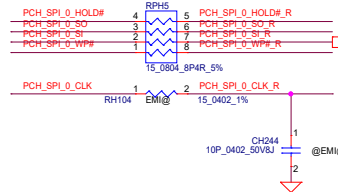
PEG(dGPU)  
SSD2  
NA  
Thunderbolt  
LAN  
WLAN  
Caldera  
SSD1

RH1 close to UH4

#571182\_CNL\_PCH\_H\_EDS\_V1\_Rev0.7  
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.  
571007\_CFL\_MOW\_Archive\_WW22\_2017  
STUFF R on GPP\_H15

Internal pull high 20K, if used qual mode need 1K pull high  
PCH\_SPI\_0\_WP#  
PCH\_SPI\_0\_HOLD#

This signal has a weak internal pull-down.  
0 = Master Attached Flash Sharing (MAFS) enabled (Default)  
1 = Slave Attached Flash Sharing (SAFS) enabled.  
Notes:  
1. This signal is in the primary well.  
Warning: This strap must be configured to 0 if the SPI or LPC strap is configured to 0.



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JIO left JUSB3  
Caldera

JUSB3 left side (Power Share, Debug Port)  
JIO right side (IO/B) USB1\_2.0  
Caldera  
AlienFX/ELC

Digital camera  
JIO right side (IO/B) USB2\_2.0  
Tobii (17" only)  
Per key  
Thunderbolt PD

BT

M.2 SSD Slot#1

X'tal Input:  
High: Differential  
Low: Single ended

JUSB2  
JUSB1

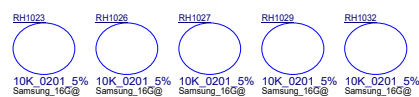
FOR SSD

	Hynix_8G	Hynix_16G	Samsung_8G	Samsung_16G	Micron_8G	Micron_16G
DDRID_0	L	H	H	H	L	H
DDRID_1	L	L	H	H	L	L
DDRID_2	L	L	L	L	H	H
DDRID_3	L	L	L	L	L	L
DDRID_4	L	L	L	L	L	L

## Samsung\_8G



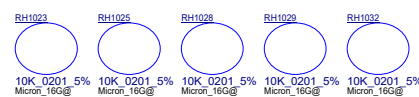
## Samsung\_16G



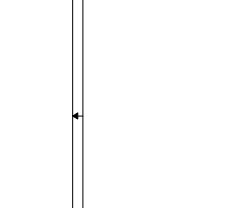
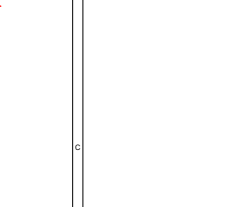
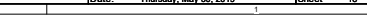
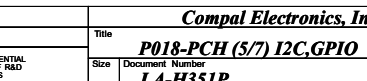
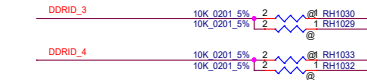
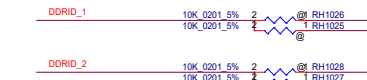
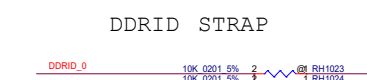
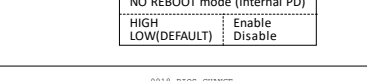
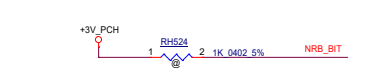
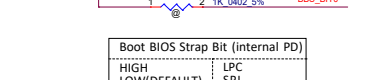
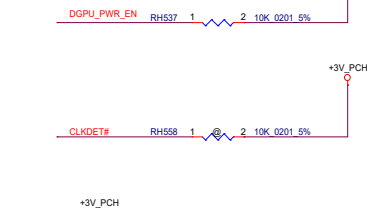
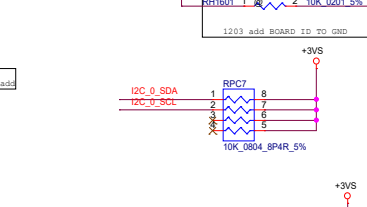
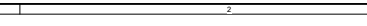
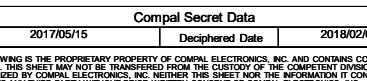
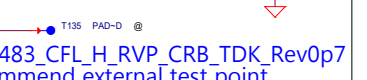
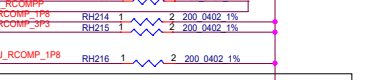
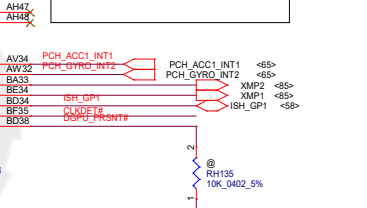
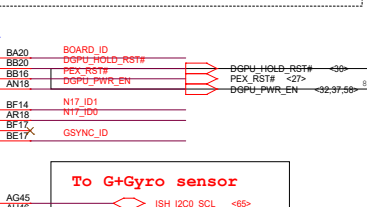
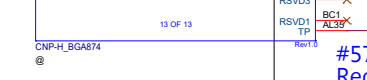
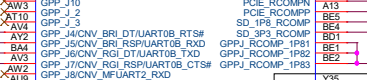
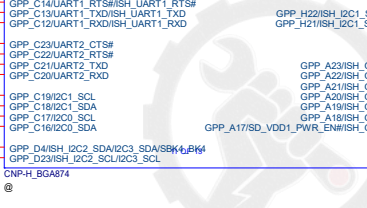
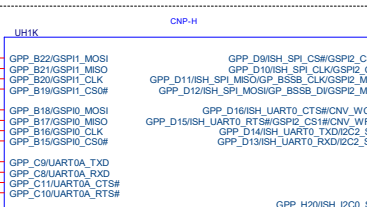
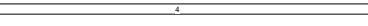
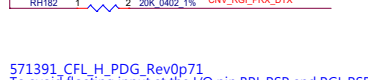
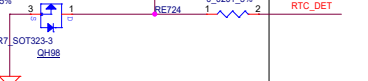
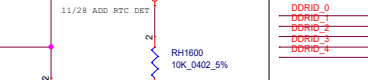
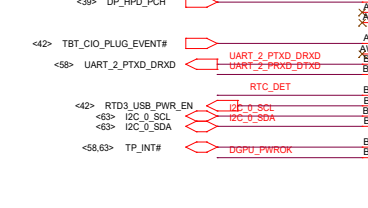
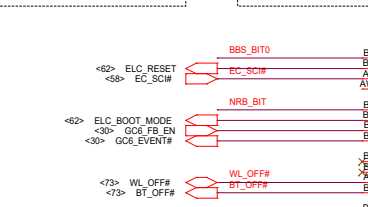
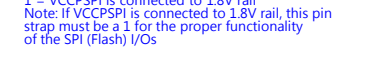
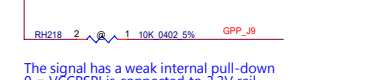
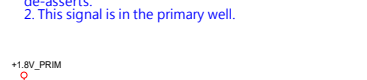
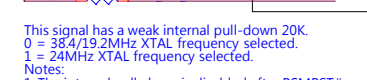
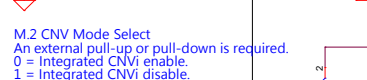
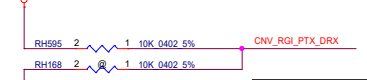
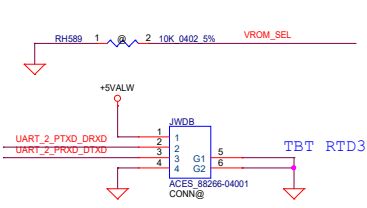
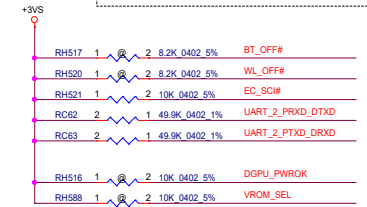
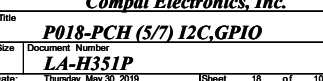
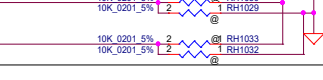
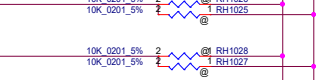
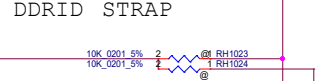
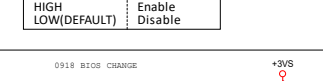
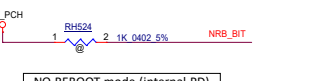
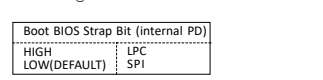
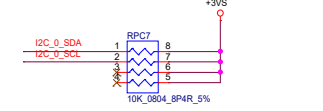
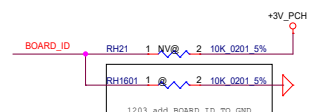
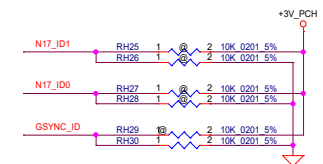
## Micron\_8G



## Micron\_16G



nVidia GPU_ID	N18_ID1	N18_ID0
N18EG3	H	H
N18EG2	H	L
N18EG1	L	H
N18EG0	L	L



The signal has a weak internal pull-down  
0 = VCCPSPI is connected to 3.3V rail  
1 = VCCPSPI is connected to 1.8V rail  
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a 1 for the proper functionality of the SPI (Flash) I/Os

571391\_CFL\_H\_PDG\_Rev0p71  
To avoid floating input at the I/O pin BRI\_RSP and RGI\_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

571483\_CFL\_H\_RVP\_CRB\_TDK\_Rev0p7  
Recommend external test point

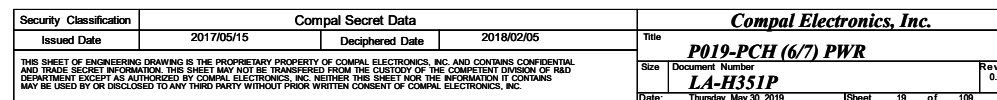
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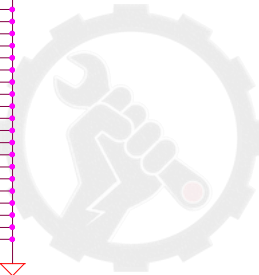
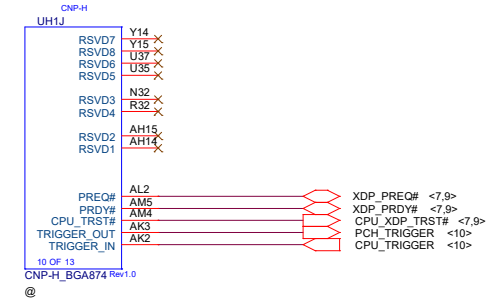
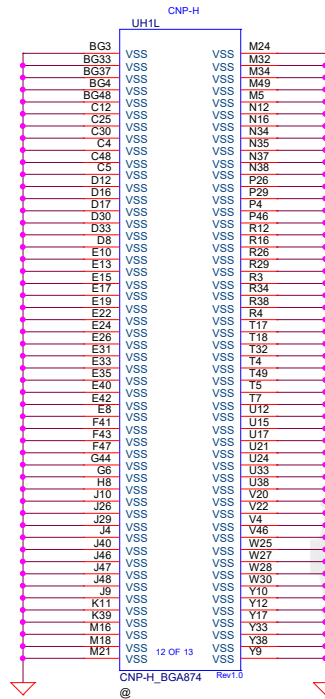
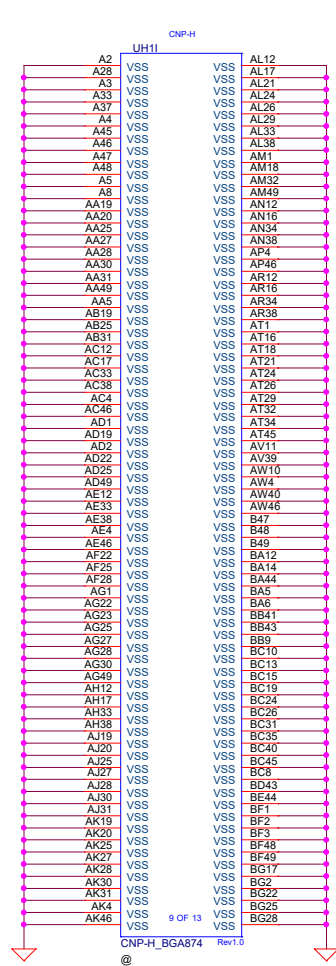
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Recommend external test point

571483\_CFL\_H\_RVP\_CRB\_TDK\_Rev0p7  
Recommend external test point

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P021-Reserve			
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				A
Title				
P022-Reserve				
Size	Document	Number	Rev	
A	LA-H351P		0.1	
Date:	Thursday, May 30, 2019		Sheet	22 of 109

DDR4 Memory Down\_CHA

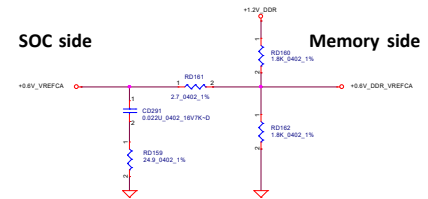
Non-Interleave Memory



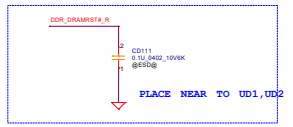
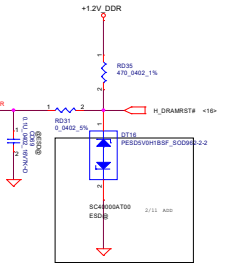
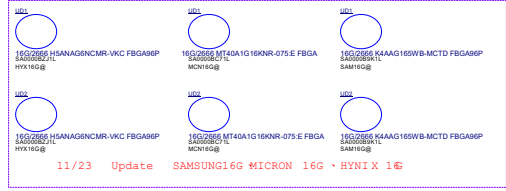
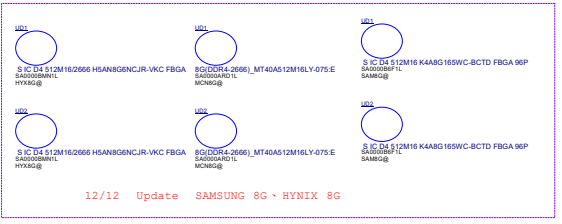
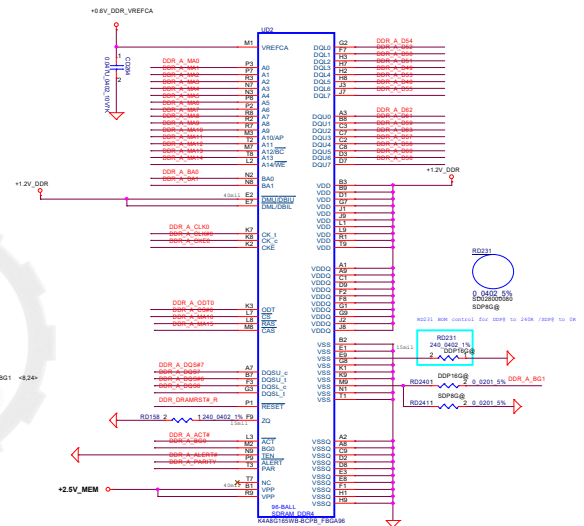
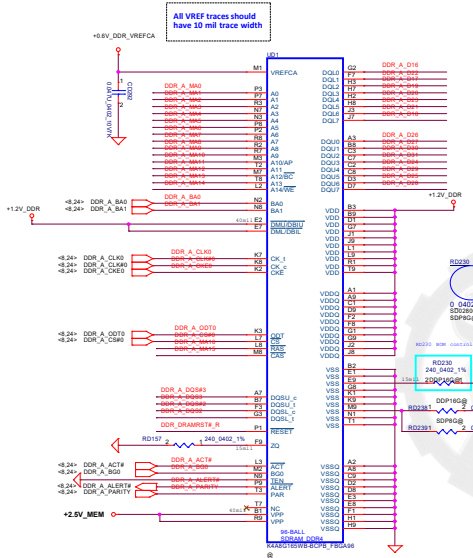
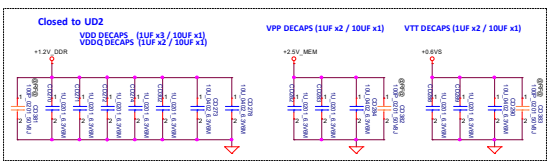
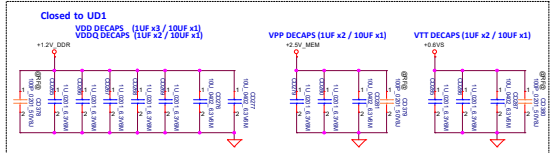
DDR4 Memory Down\_CHA

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SOC side Memory side



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.

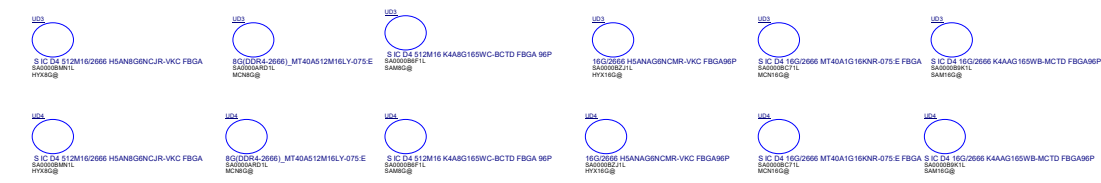
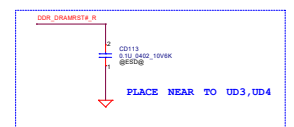
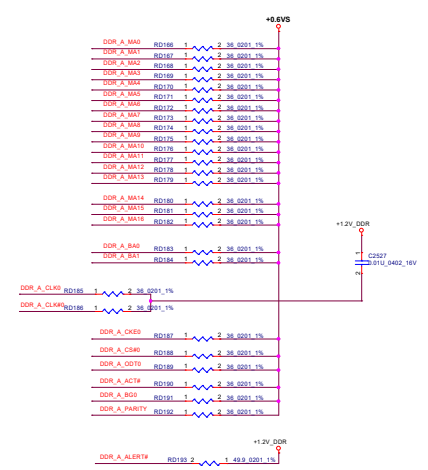
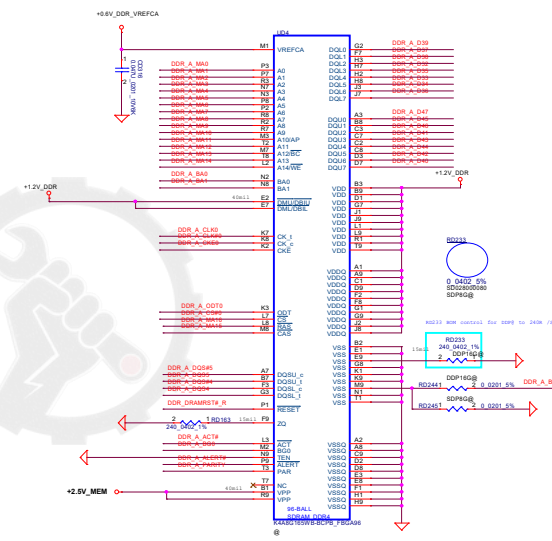
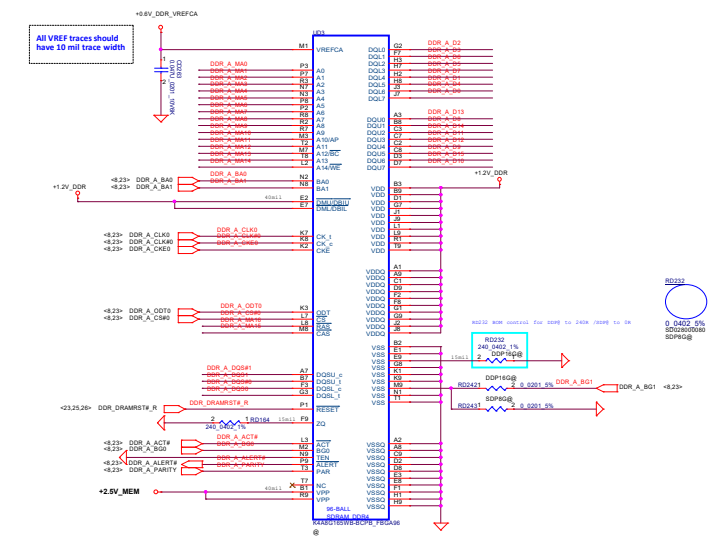
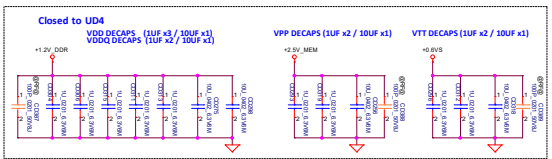
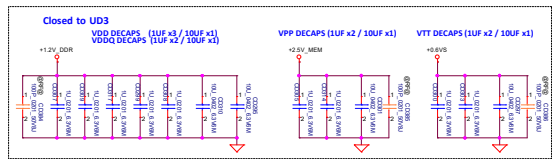


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A4				LA-H351P	
Date				Sheet	
Thursday, May 24, 2019				21 of 100	

DDR4 Memory Down\_CHA  
Non-Interleave Memory

+8.25V DDR\_A\_M0[0:16]  
+8.25V DDR\_A\_D0[0:7]  
+8.25V DDR\_A\_D0[8:15]  
+8.25V DDR\_A\_D0[16:31]

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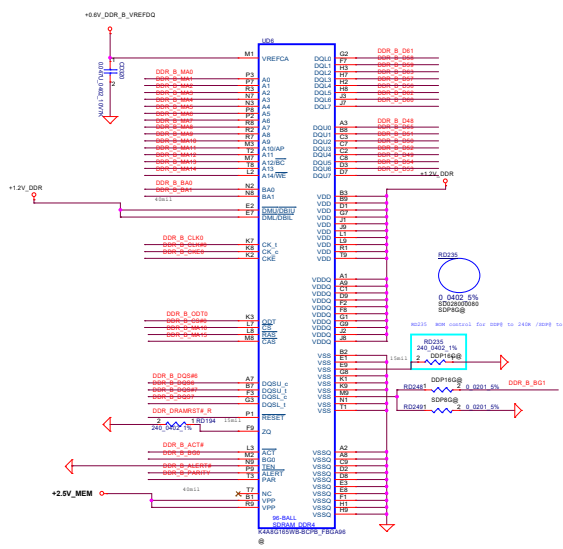
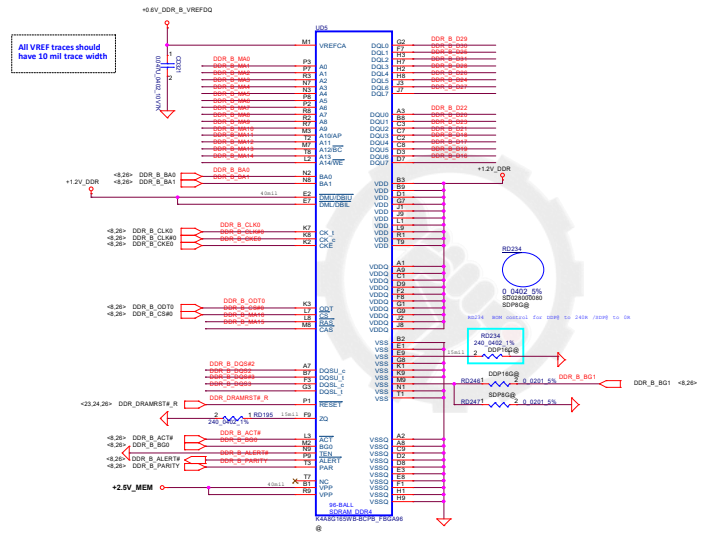
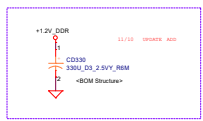
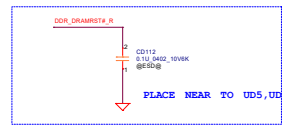
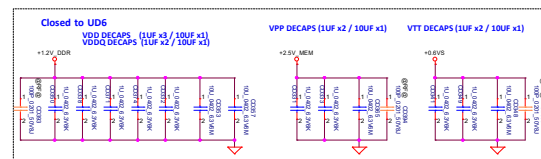
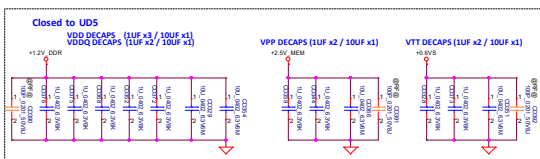
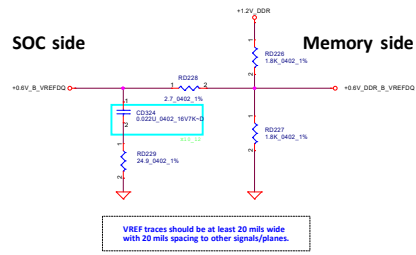
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Issued Date	2017/04/07	Declassification Date	2018/12/31	P024-DDR4 CHA Memory Down II
Rev	1	Rev	1	LA-H351P
Rev	1	Rev	1	Rev

DDR4 Memory Down\_CHB  
Non-Interleave Memory



DDR4 Memory Down\_CHB

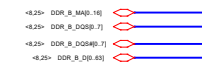
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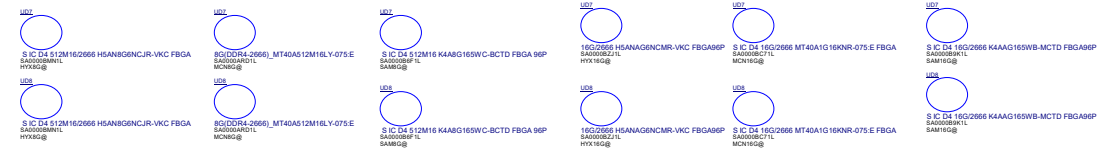
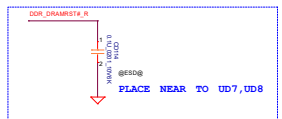
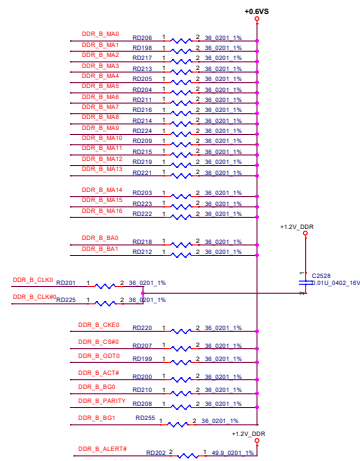
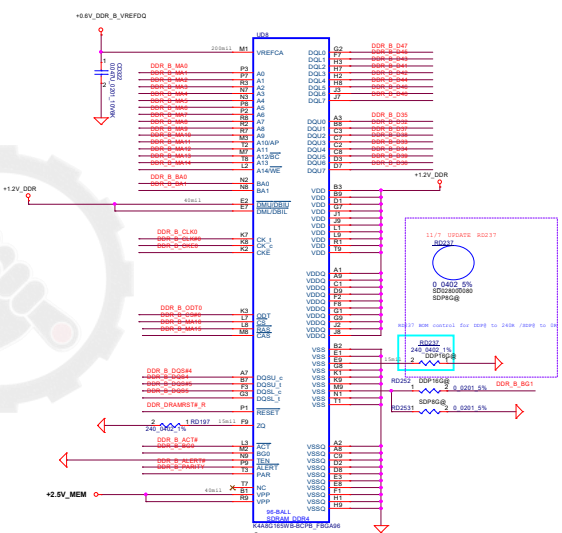
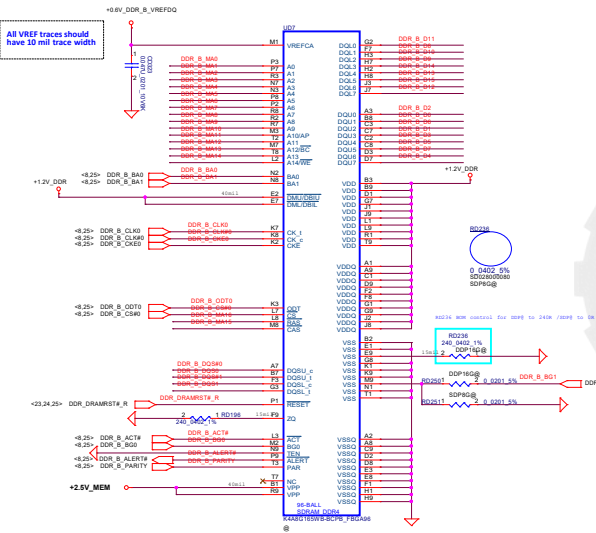
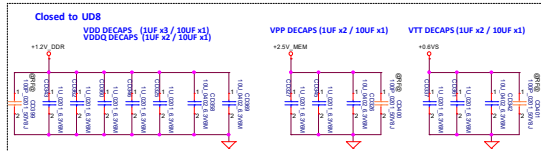
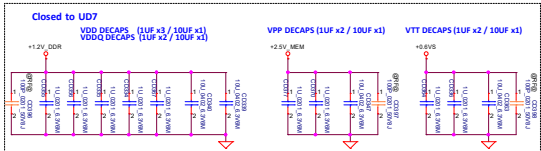
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U0A	U0A	U0A	U0A	U0A	U0A
S IC D4 912M16/2666 H5ANBGNC-JR-VKC FBGA SAG0089T1L HYX08@	S IC D4 912M16/2666 H5ANBGNC-JR-VKC FBGA SAG0089T1L HYX08@	S IC D4 912M16/2666 H5ANBGNC-JR-VKC FBGA SAG0089T1L HYX08@	S IC D4 912M16/2666 H5ANBGNC-JR-VKC FBGA SAG0089T1L HYX08@	S IC D4 912M16/2666 H5ANBGNC-JR-VKC FBGA SAG0089T1L HYX08@	S IC D4 912M16/2666 H5ANBGNC-JR-VKC FBGA SAG0089T1L HYX08@

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COMPAQ ELECTRONICS, INC. P025-DDR4 CHB Memory Down I LA-H351P			

DDR4 Memory Down\_CHB  
Non-Interleave Memory



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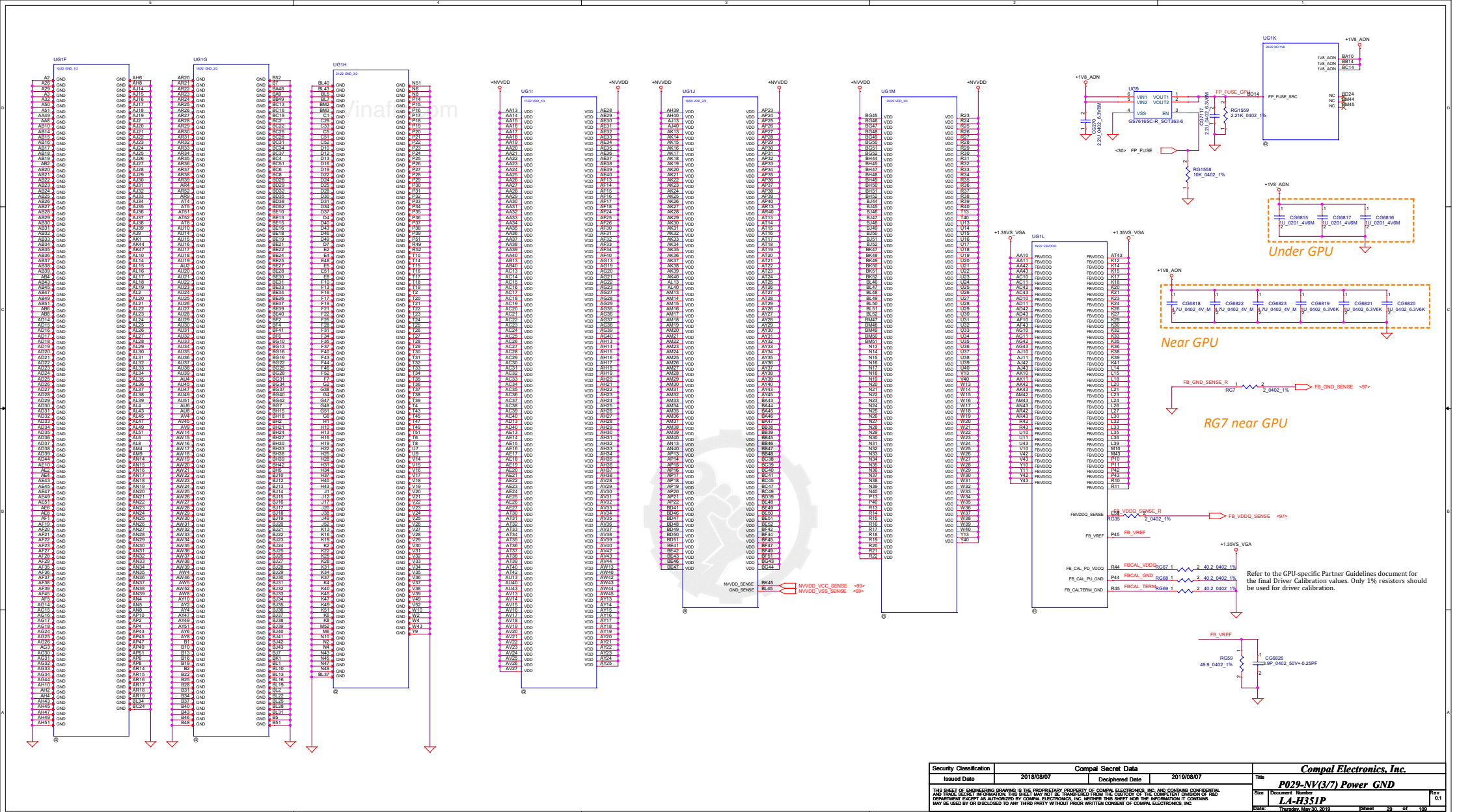


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LA-H351P				Rev 0.1	
Date: 2019.09.23.2019				Sheet 25 of 100	

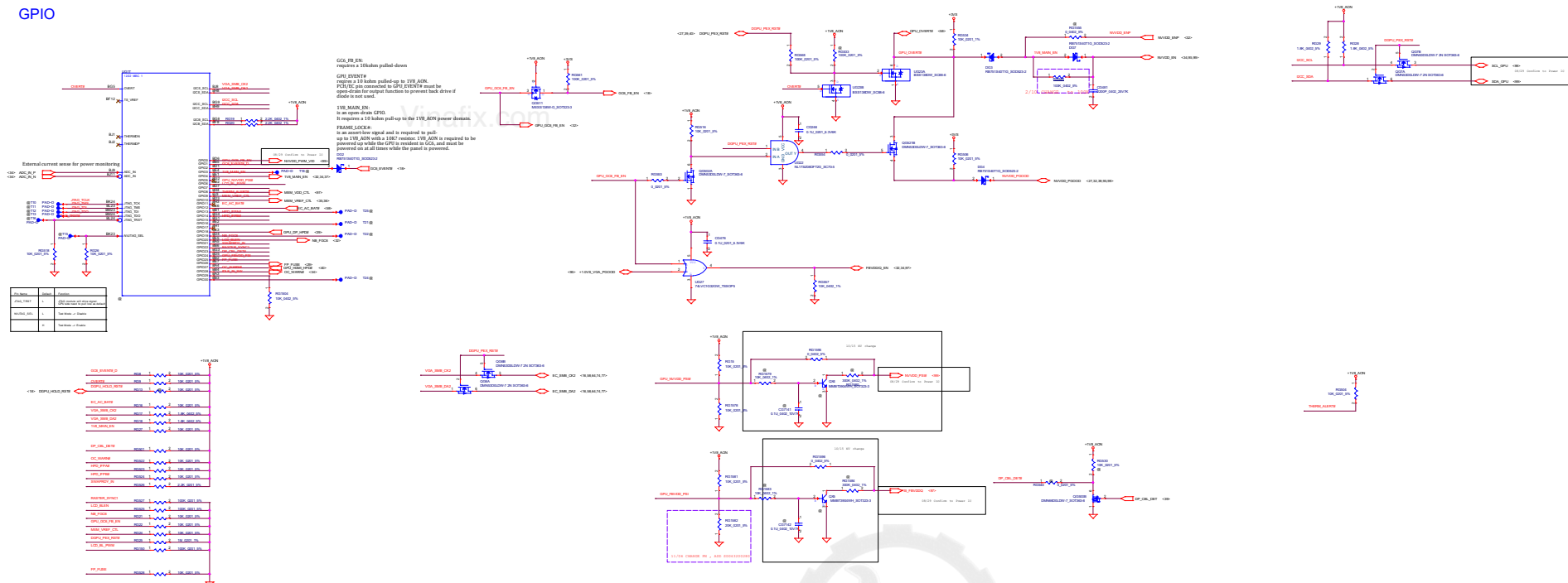




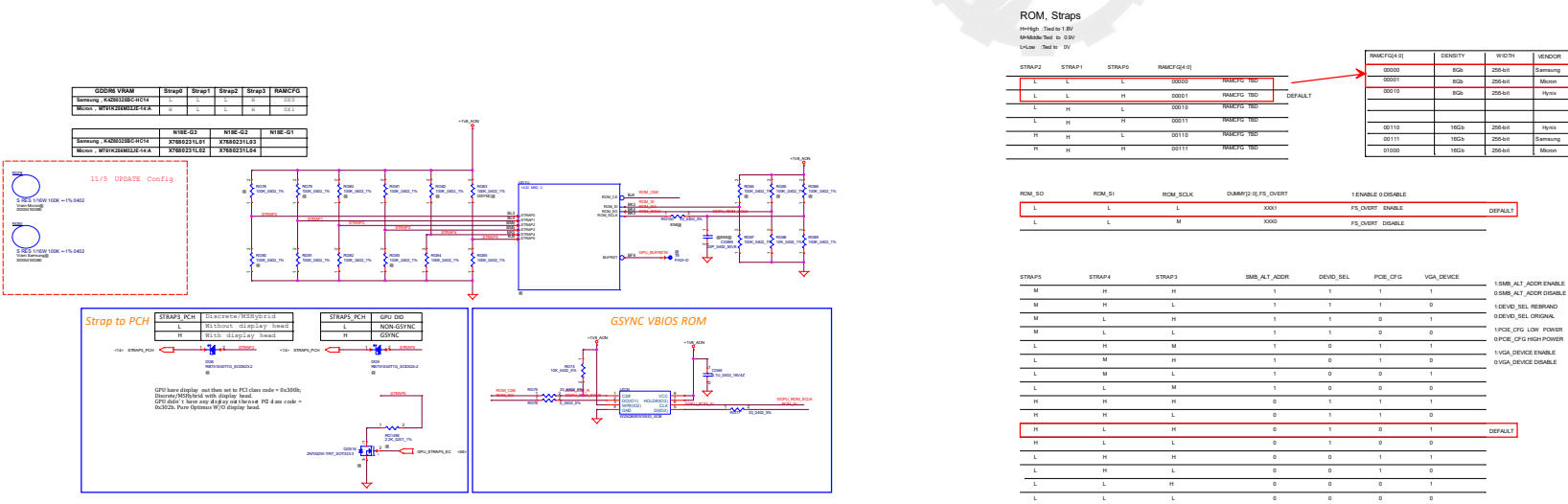


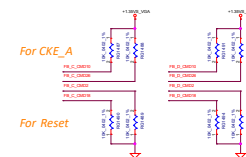
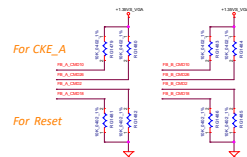
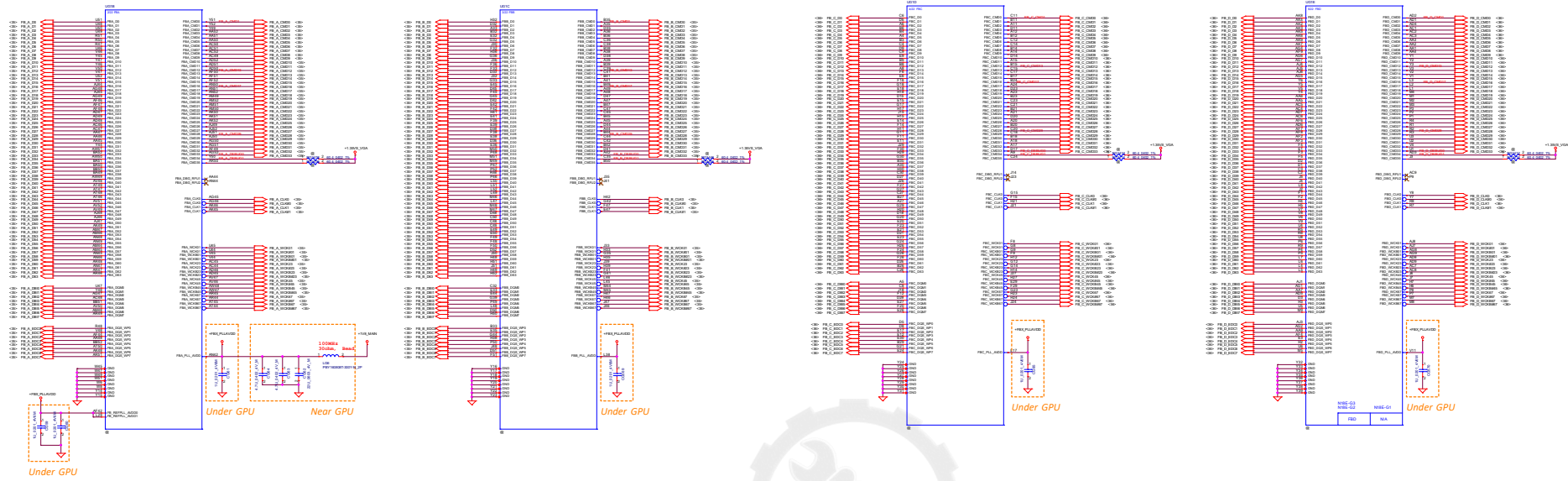


## GPIO



## BIOS STRAP

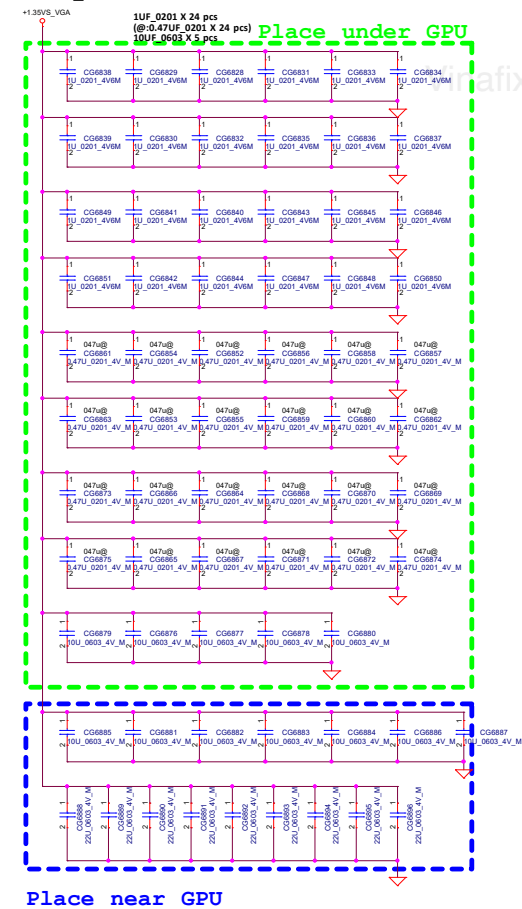






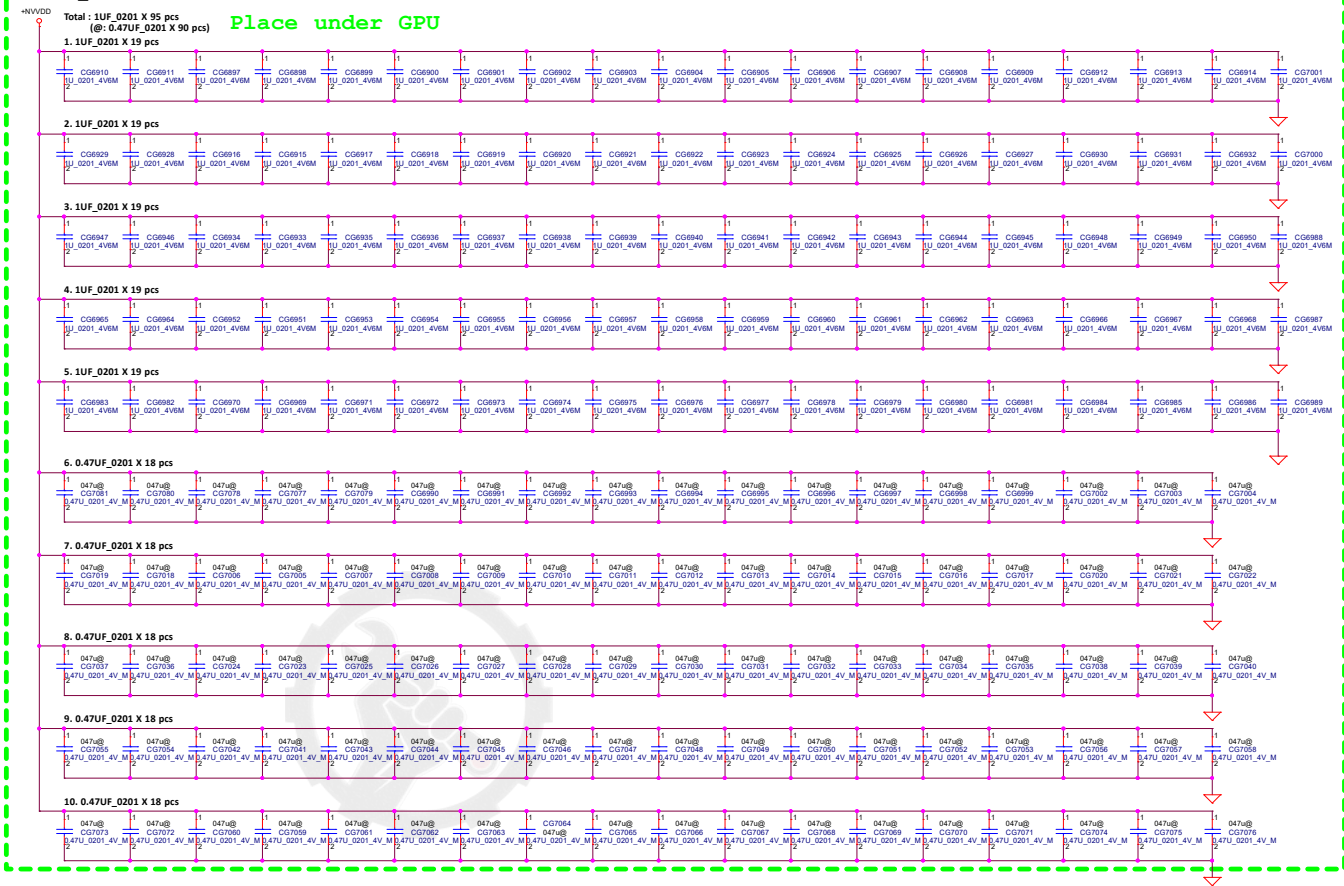
GPU Decoupling - NV Spec Recommendation

FBVDDQ\_GPU



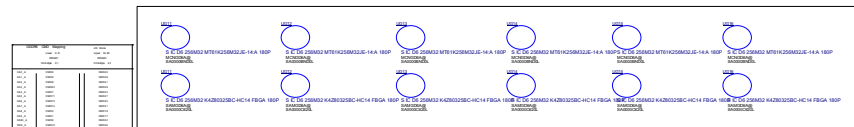
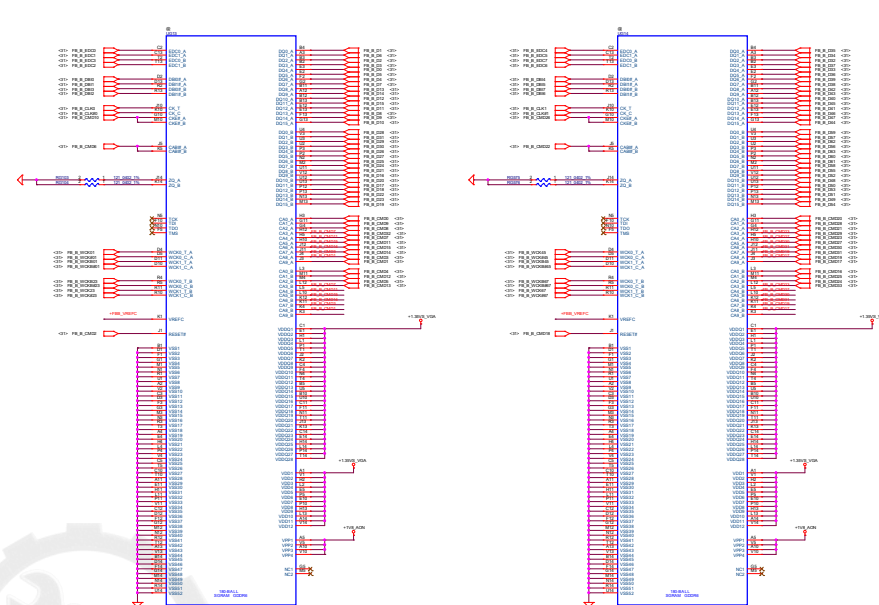
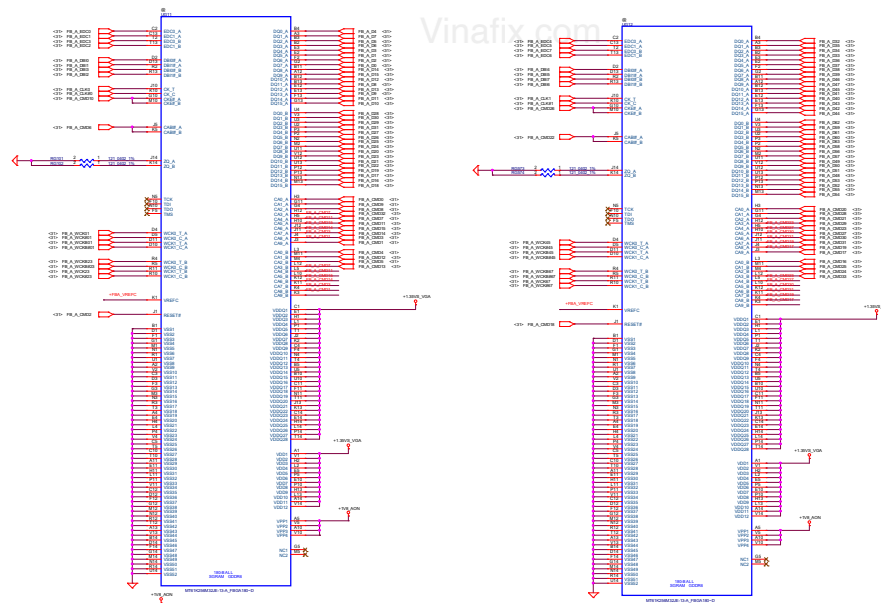
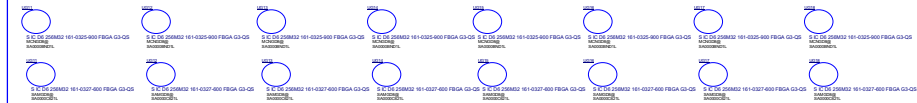
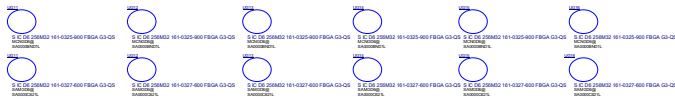
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0.47UF\_0201 X 90 pcs

NVVDD\_GPU

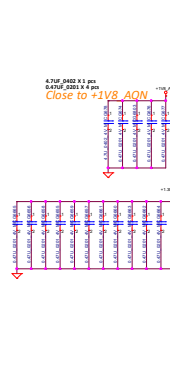
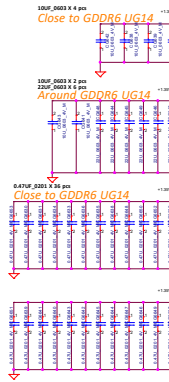
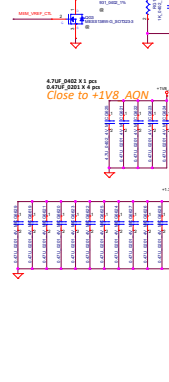
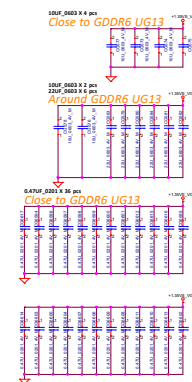
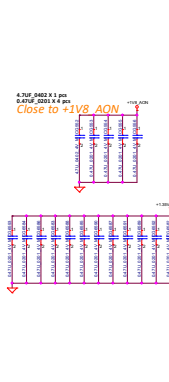
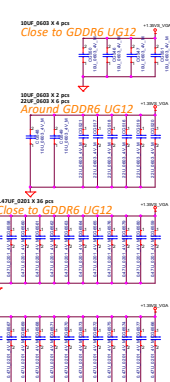
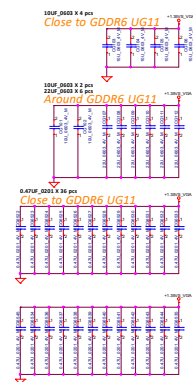
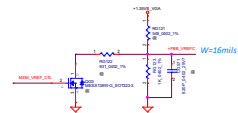
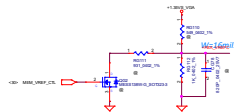


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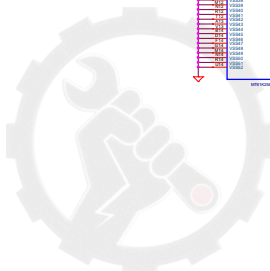
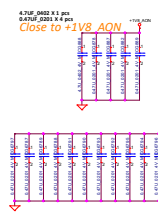
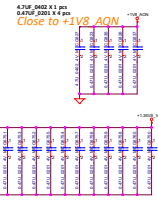
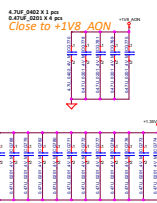
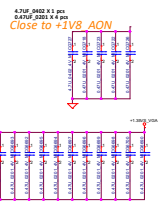
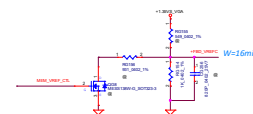




Rev	By	Date	Description
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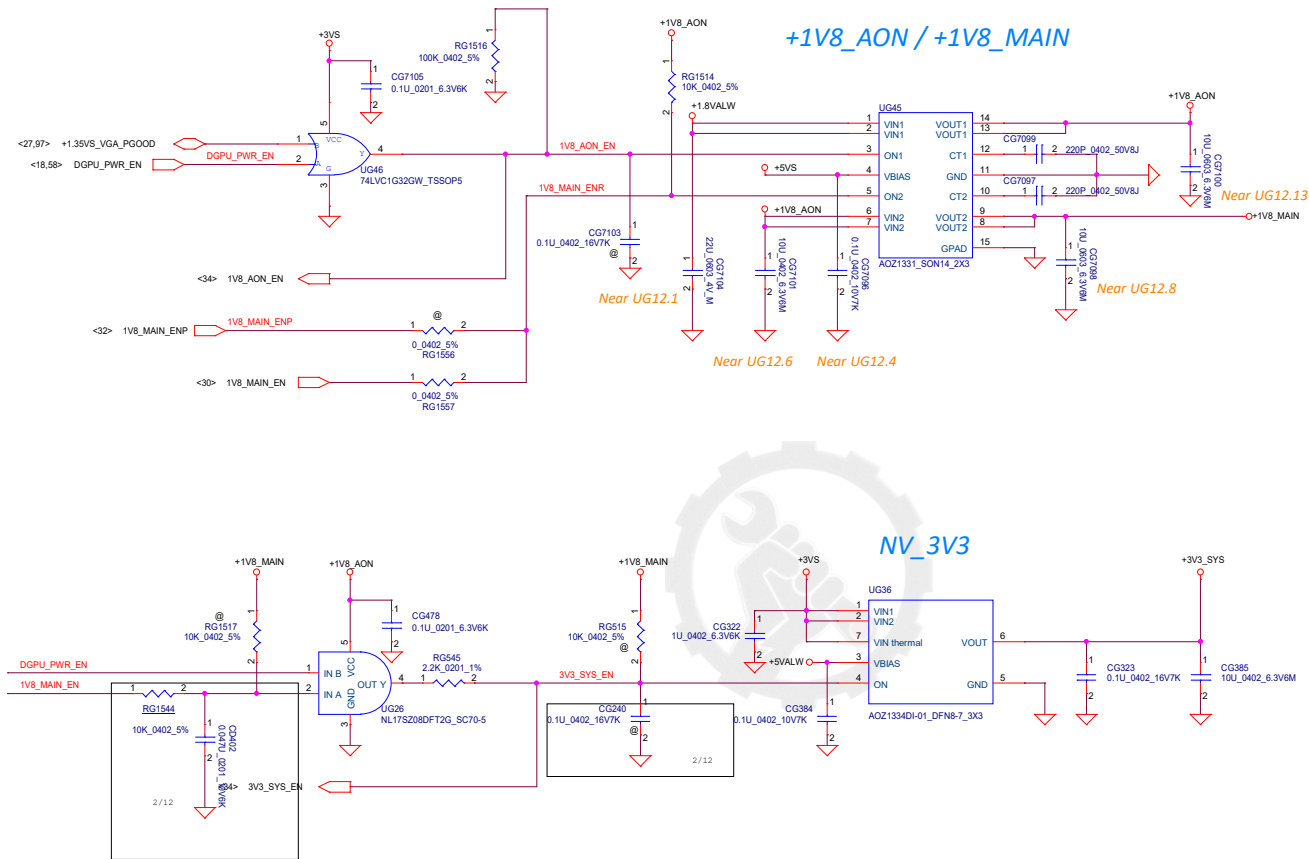




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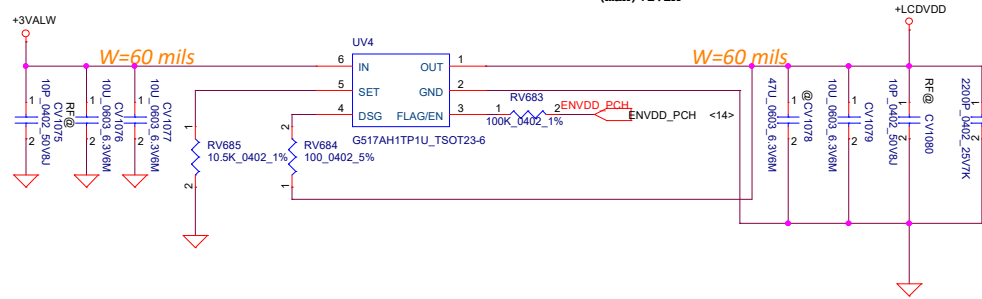
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1. 0401 --> 0201  
2. X5R --> X7R or X8R



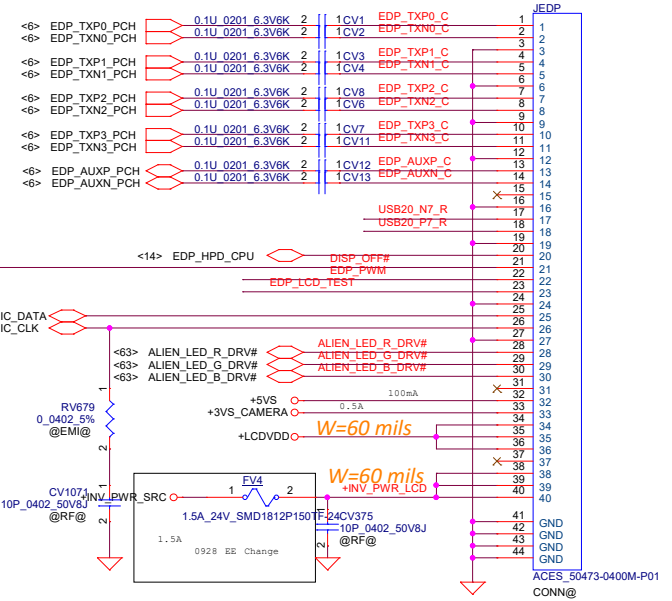


# UPDATE 0914 LCD power control

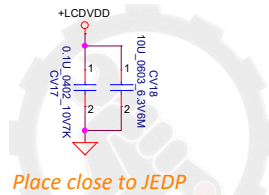
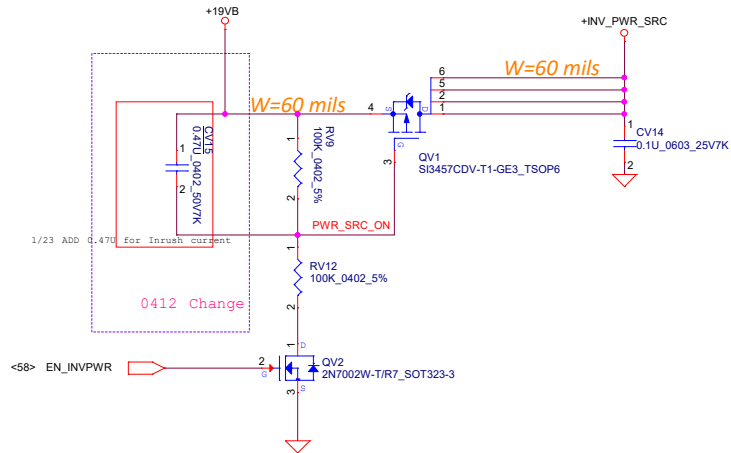
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(typ):2A  
(max):2.2A



## eDP connector

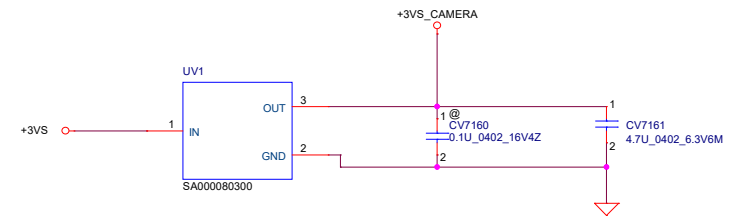


## LCD backlight power control

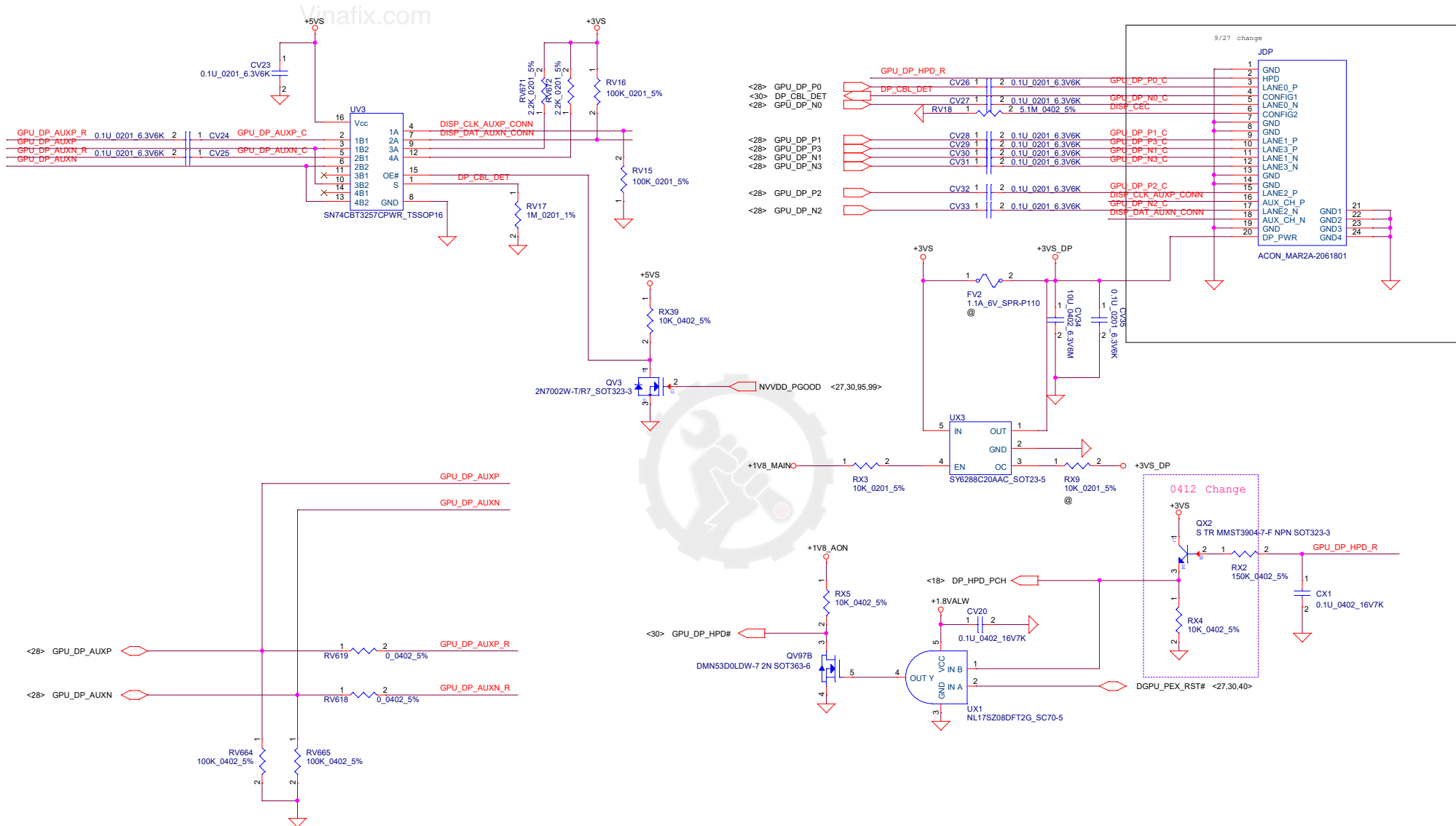


## CAMERA POWER

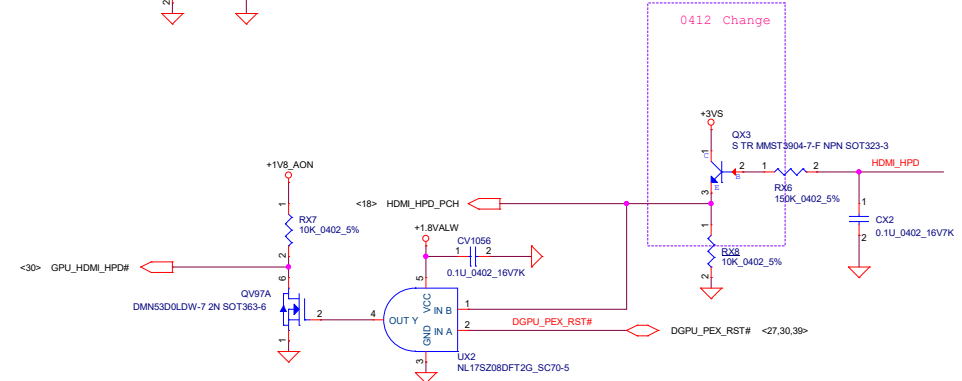
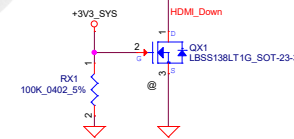
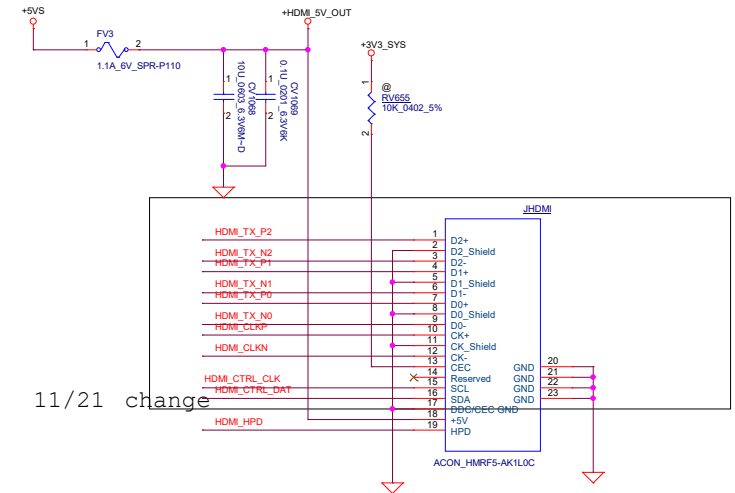
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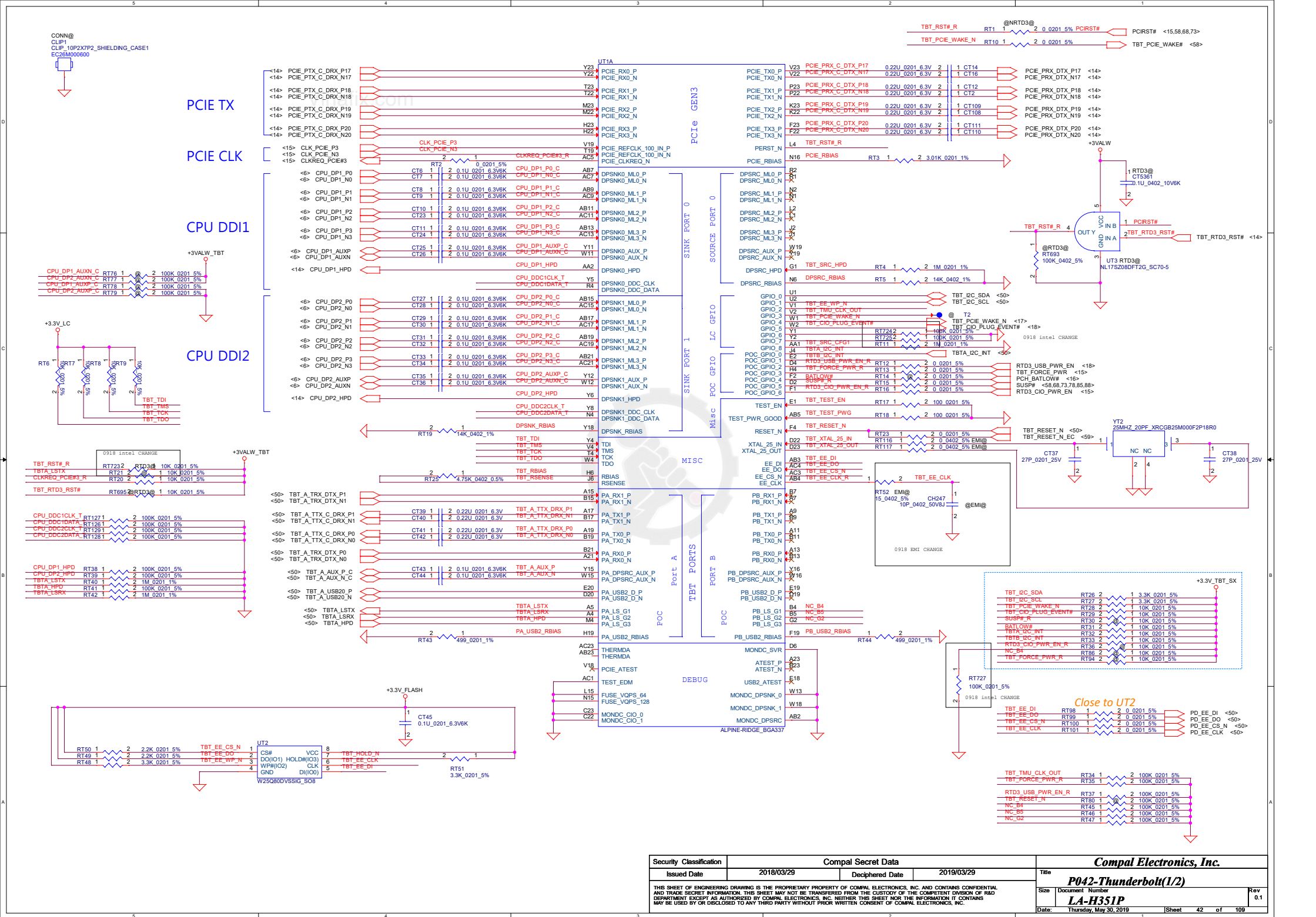


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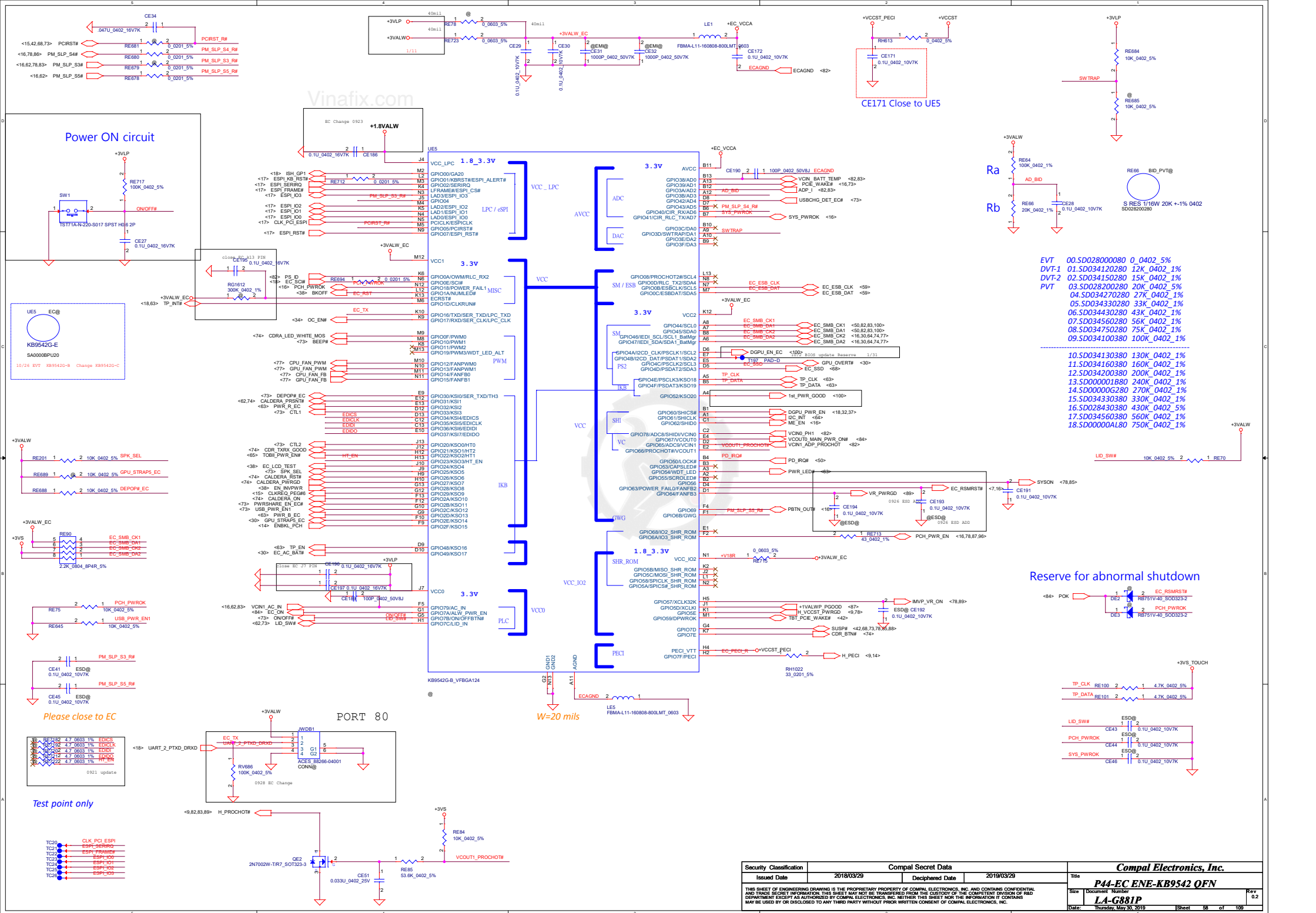


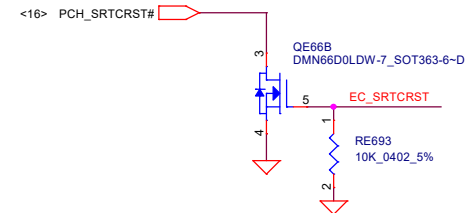
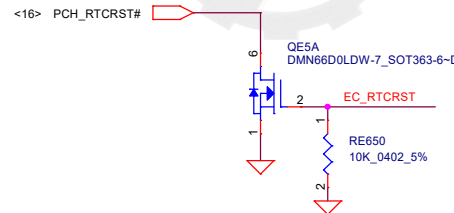
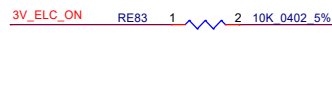
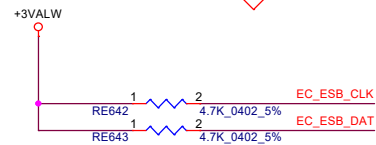
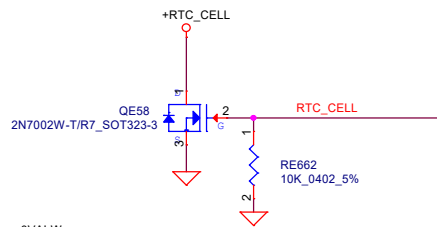
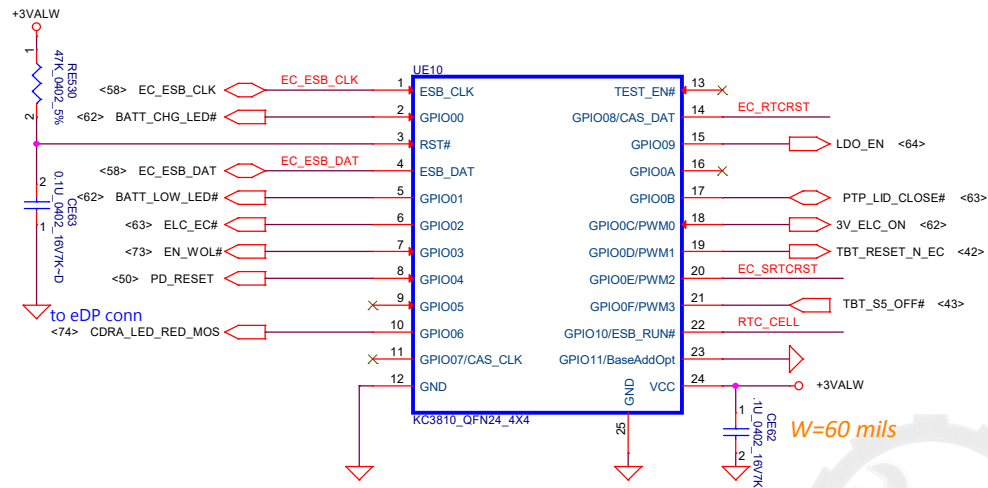
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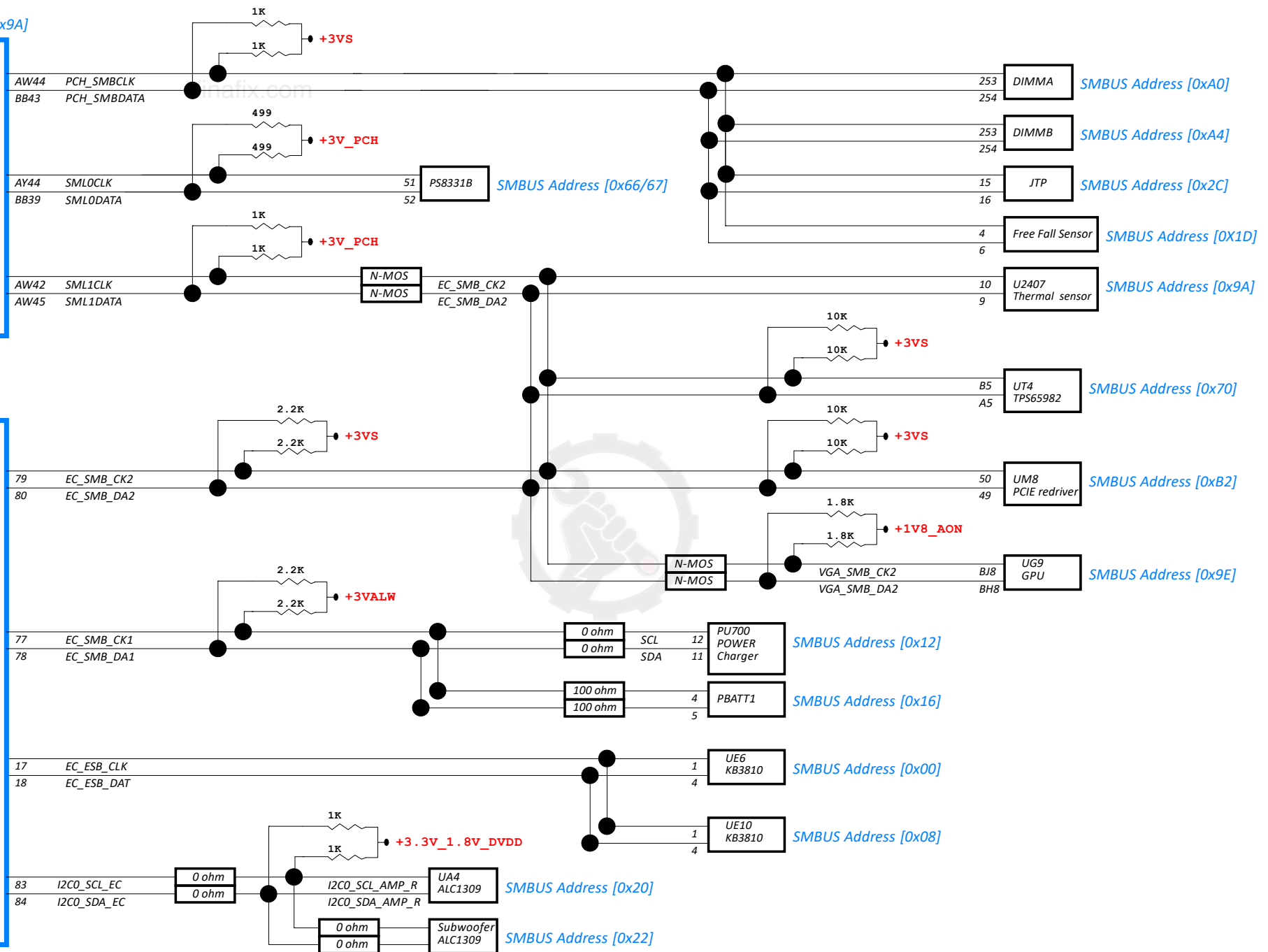
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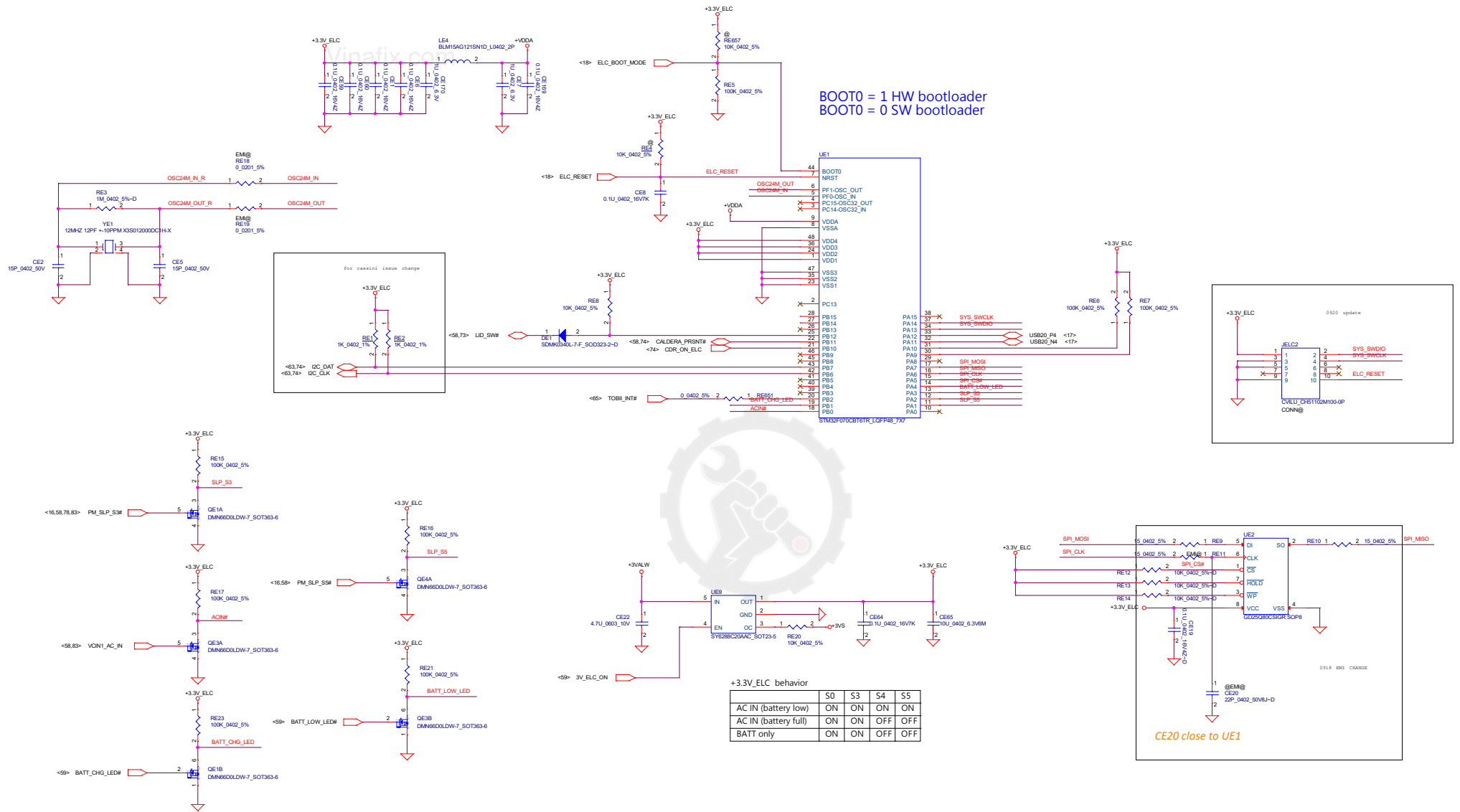
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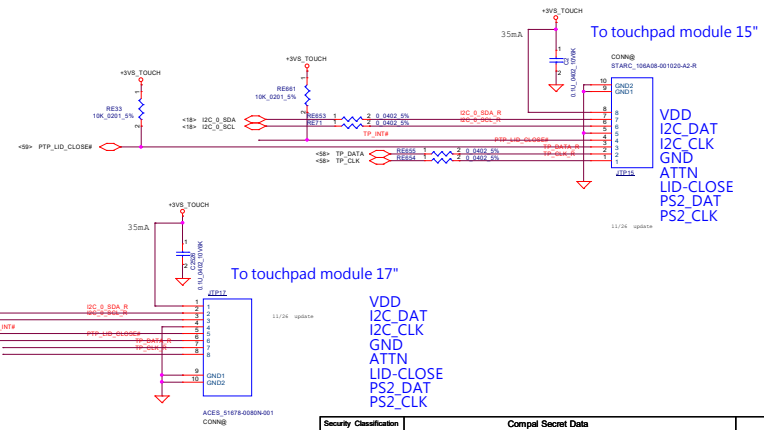
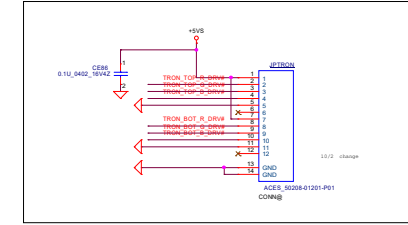
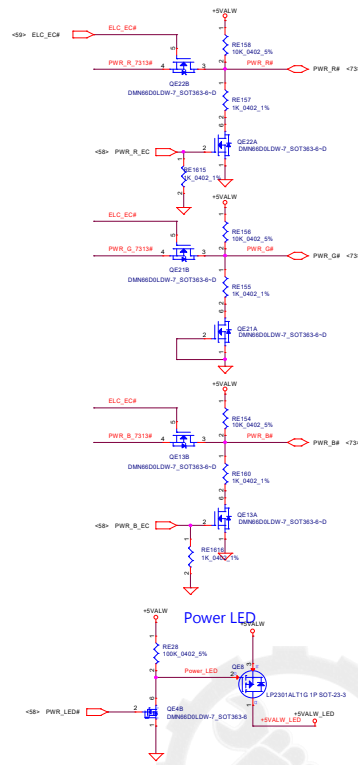
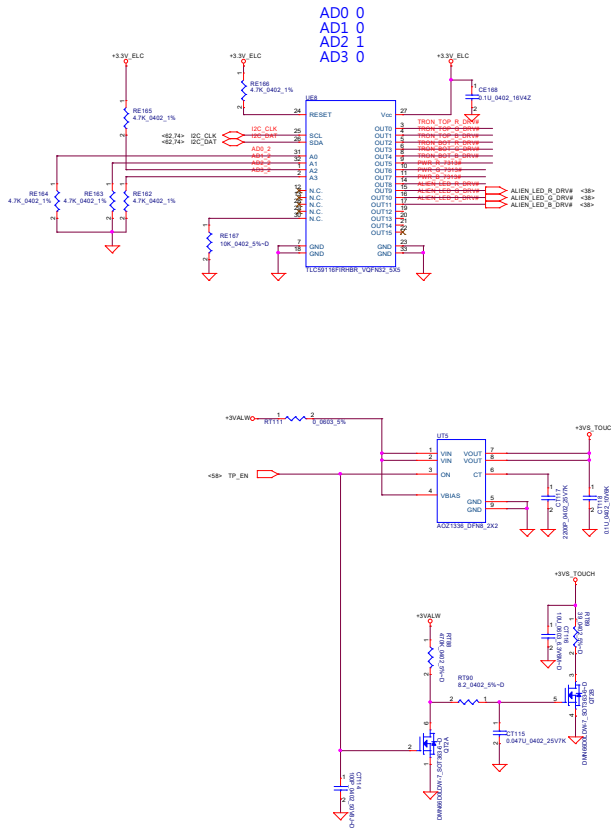
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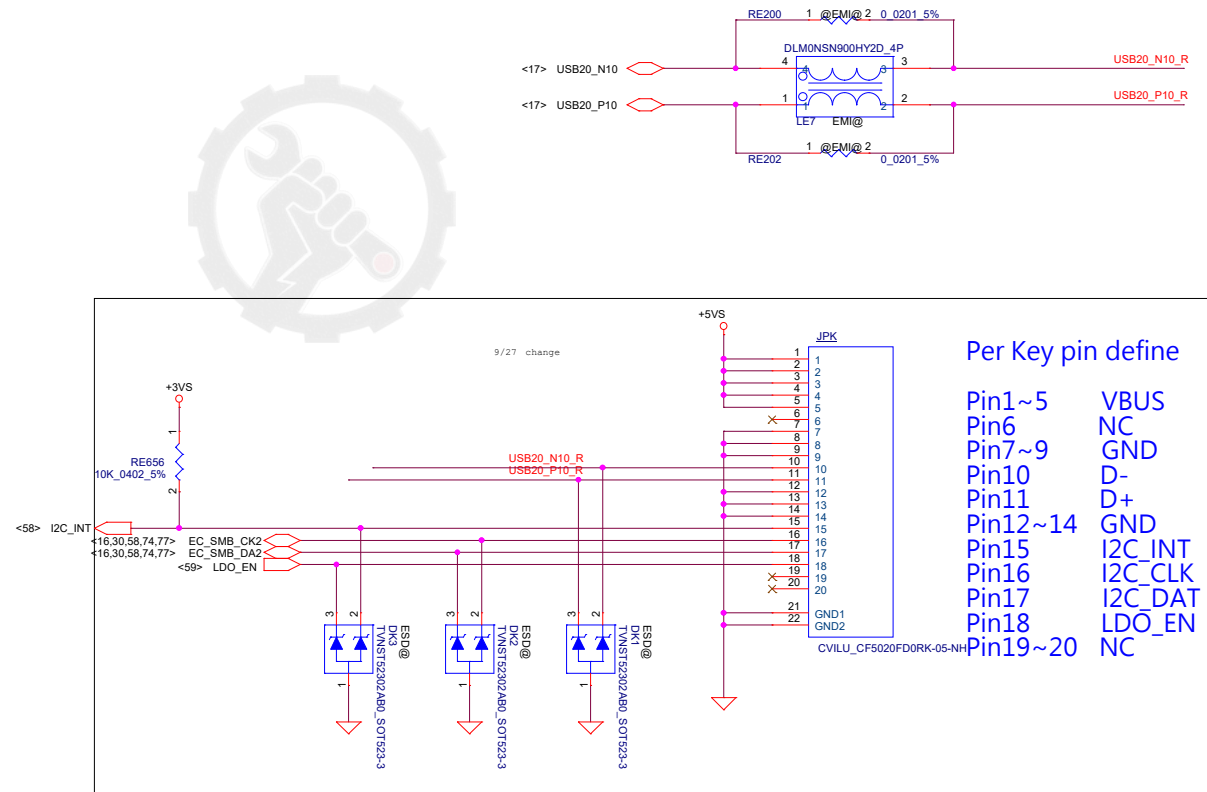


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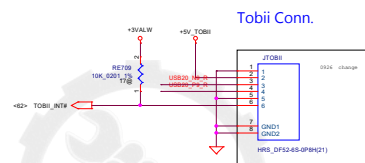
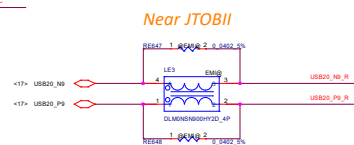
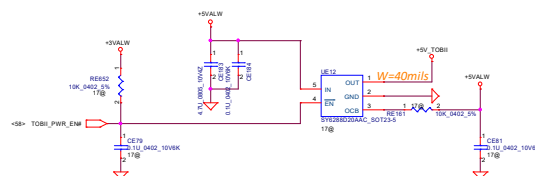
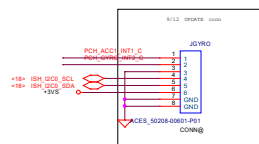




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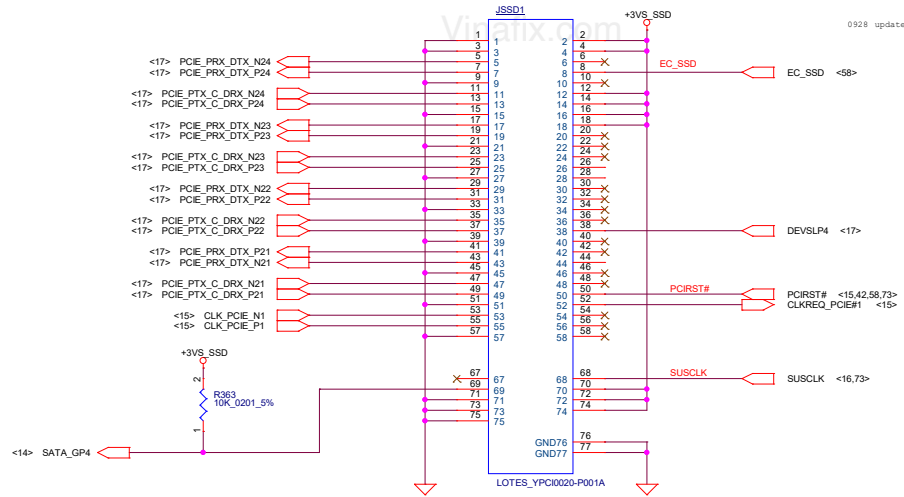


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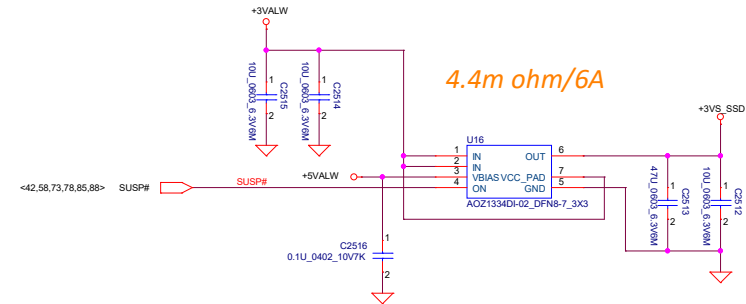
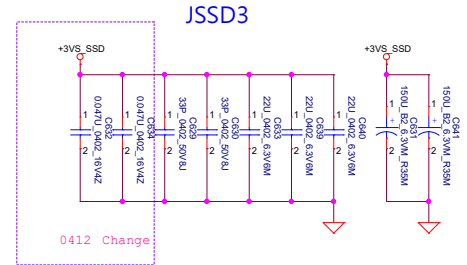
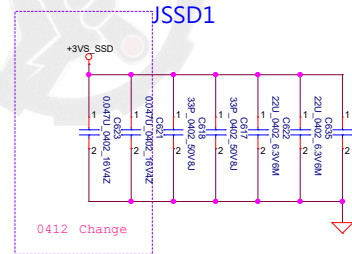
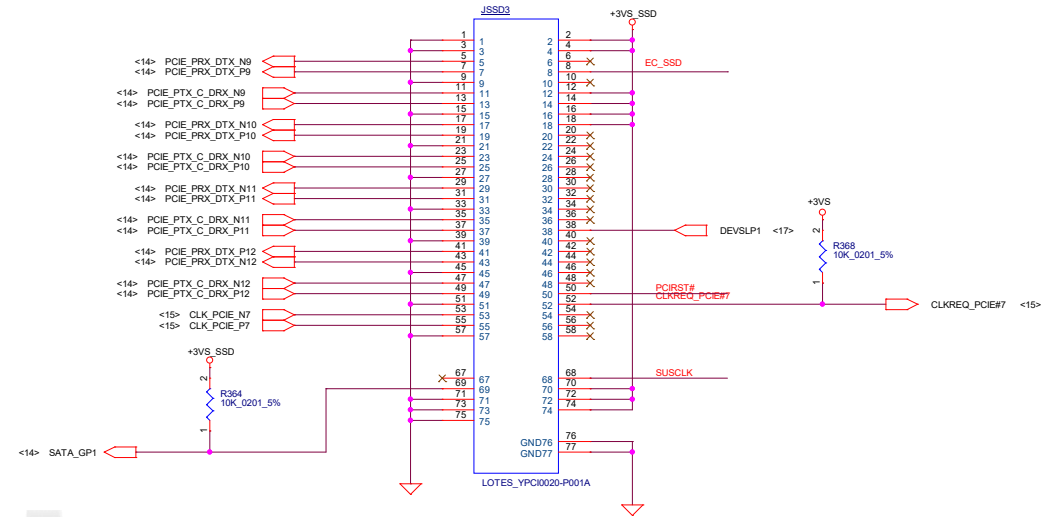
Title			
P067-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	67 of 109

PCIe  
JSSD1 , 2280



PEDET	Module Type
0	SATA
1	PCIe

PCIe / SATA SSD  
JSSD3 , 2280



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2017/05/15	Deciphered Date	2018/02/05	Title	<b>P068-NGFF SSD</b>	
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				<b>LA-H351P</b>		
				Date:	Thursday, May 30, 2019	Sheet 68 of 109



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Title			
P069-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	69 of 109

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Title			
P070-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	70 of 109

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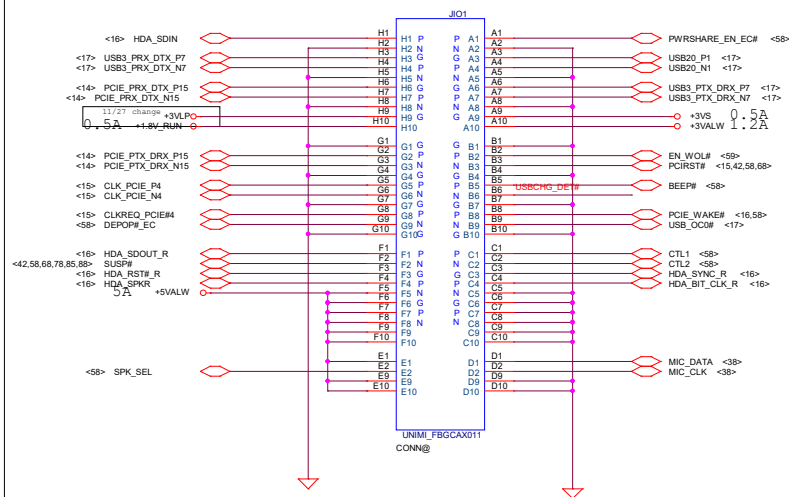
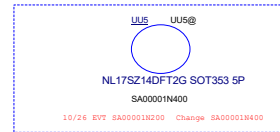
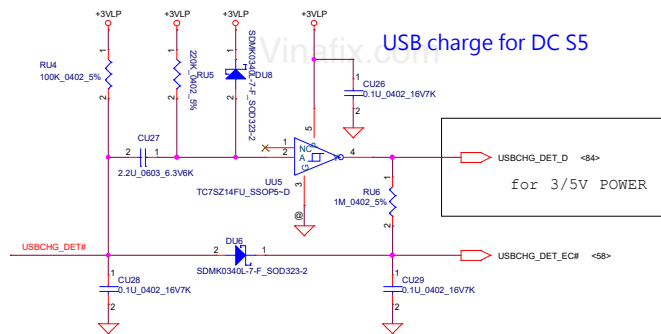


Title			
P071-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	71 of 109

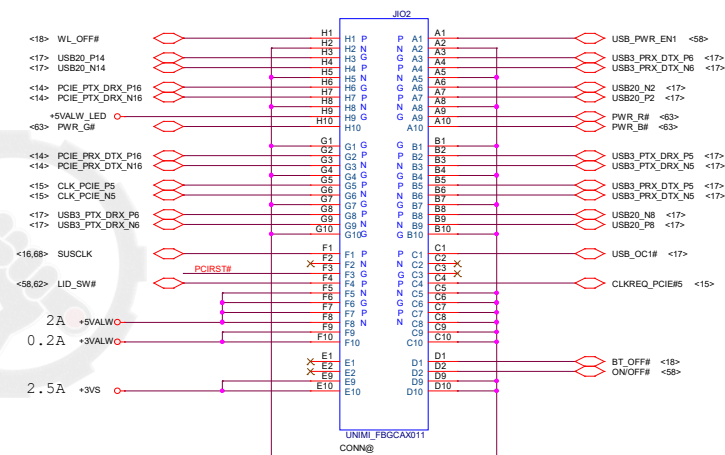
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Title			
P072-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
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For Audio DB conn



For USB DB conn

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Size	Document	Number	Rev	LA-H351P	
Date:	Thursday, May 30, 2019	Sheet	73	of	109



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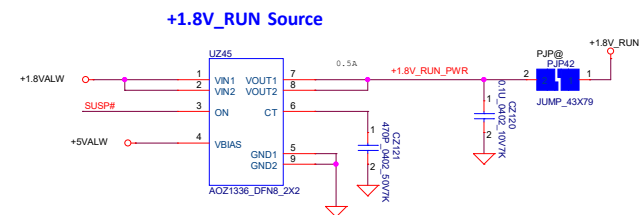
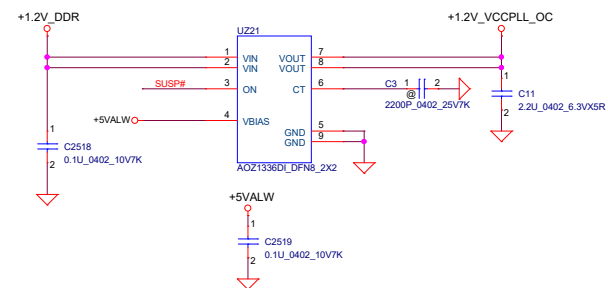
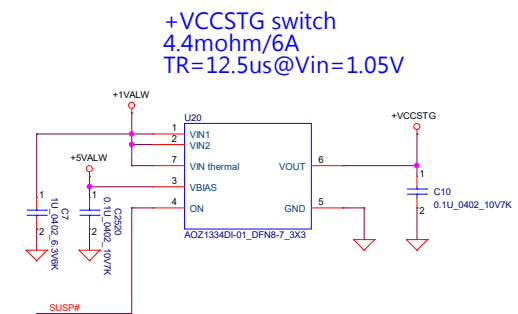
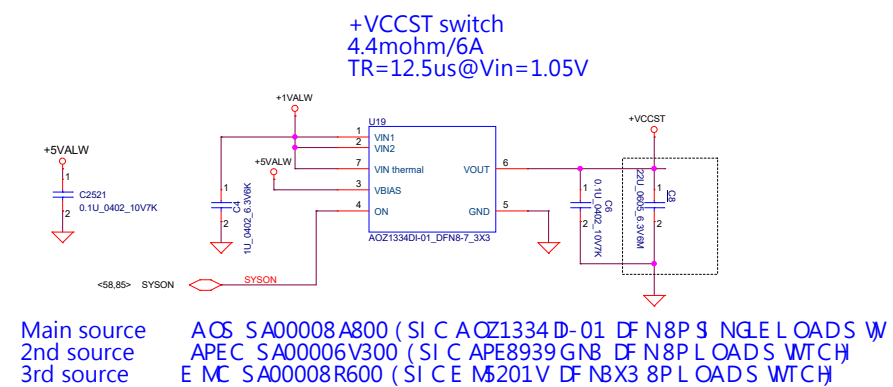
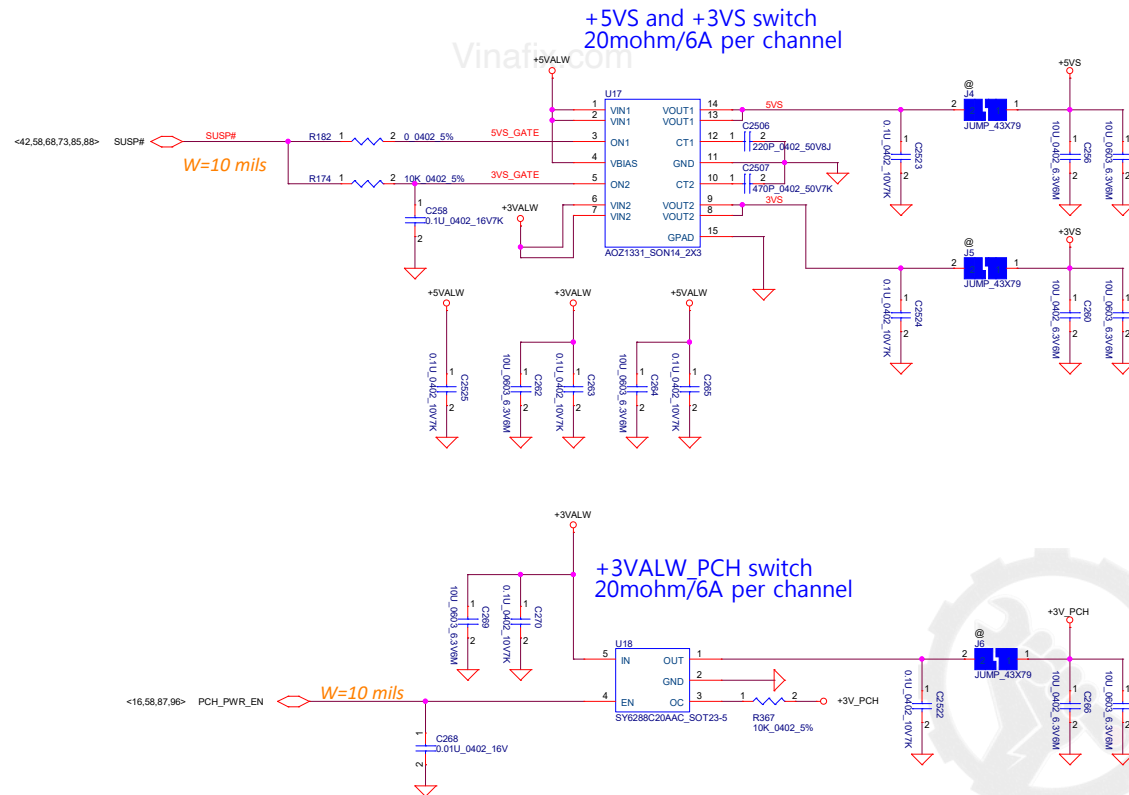
Title			
P075-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	75 of 109



Title			
P076-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	76 of 109





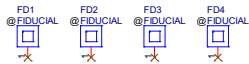


Vinafix.com

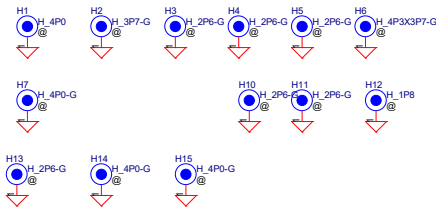


Title			
P079-Reserve			
Size	Document Number		Rev
A	LA-H351P		0.1
Date:	Thursday, May 30, 2019	Sheet	79 of 109

Fiducial Mark

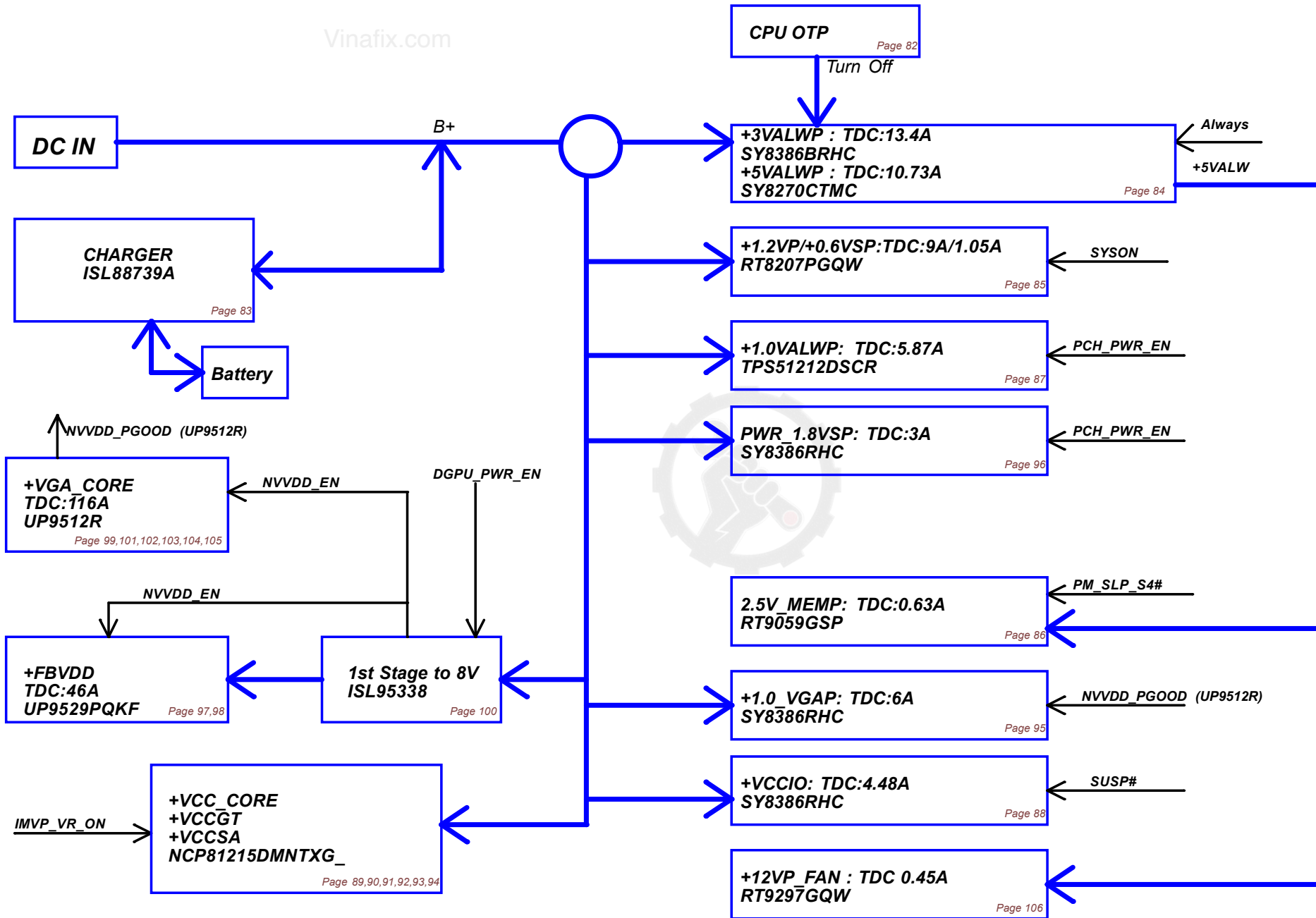


PCB Screw Hole



# Power block

Vinafix.com

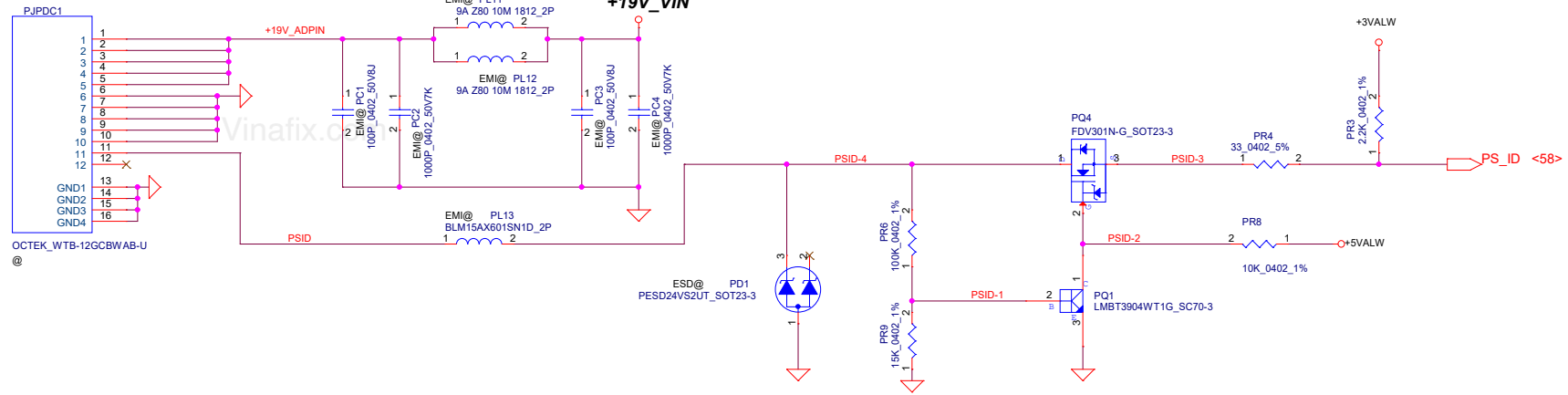


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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR POWER BLOCK DIAGRAM
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Adapter 240W  
240W/19.5V=12.31A

#### Adapter connector:

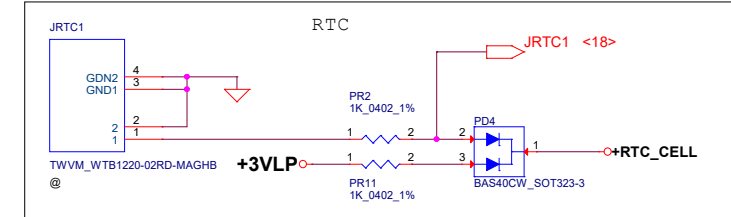
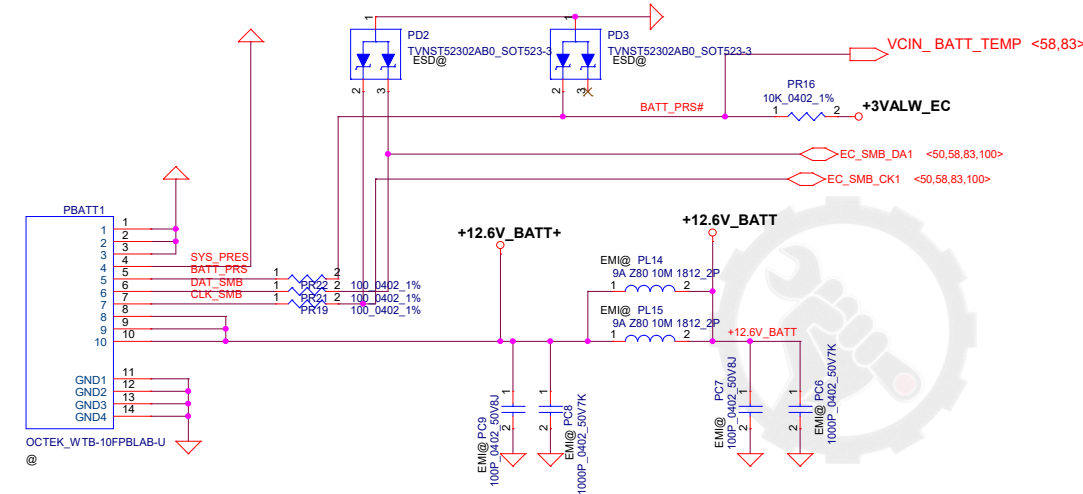
- 1.ADPIN
- 2.ADPIN
- 3.ADPIN
- 4.ADPIN
- 5.ADPIN
- 6.ADPIN
- 7.GND
- 8.GND
- 9.GND
- 10.GND
- 11.PSID
- 12.NC



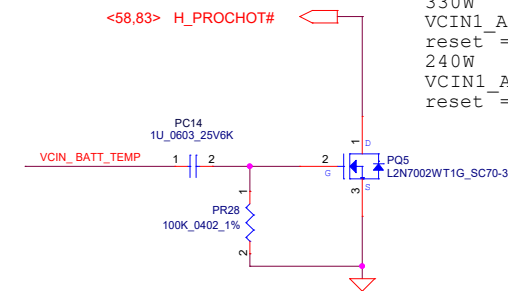
Battery 78W  
78W/11.1V=7.03A

#### Battery connector:

- 1.GND
- 2.GND
- 3.GND
- 4.SYS\_PRES
- 5.BATT\_PRS
- 6.DAT\_SMB
- 7.CLK\_SMB
- 8.BATT++
- 9.BATT++
- 10.BATT++



battery unplug procho

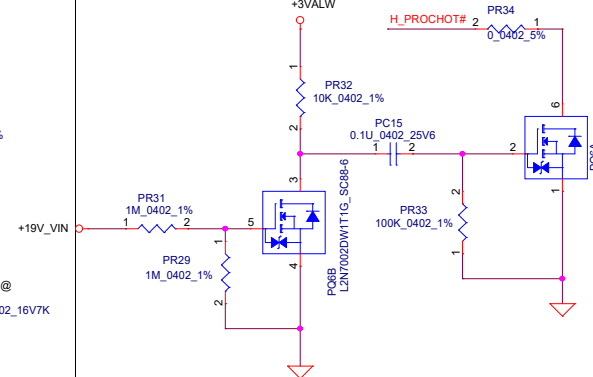


330W  
VCIN1\_ADP\_PROCHOT= 0.85V  
reset = 0.81V  
240W  
VCIN1\_ADP\_PROCHOT=0.63V  
reset = 0.59V

For PROCHOT <58> ADP\_I

<58> VCIN1\_ADP\_PROCHOT

adapter unplug procho



CPU thermal protection

VCIN0\_PH  
Trig = 1V  
93 +/- 3 degree C  
Recover = 2.28V  
50 +/- 3 degree C

<58> VCIN0\_PH1

<58> ECAGND

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/05/15	Deciphered Date	2017/01/06	Title	PWR-DCIN / BATT CONN / OTP
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				LA-F551P	Rev 1.0
				Date:	Thursday, May 30, 2019
				Sheet	82 of 109

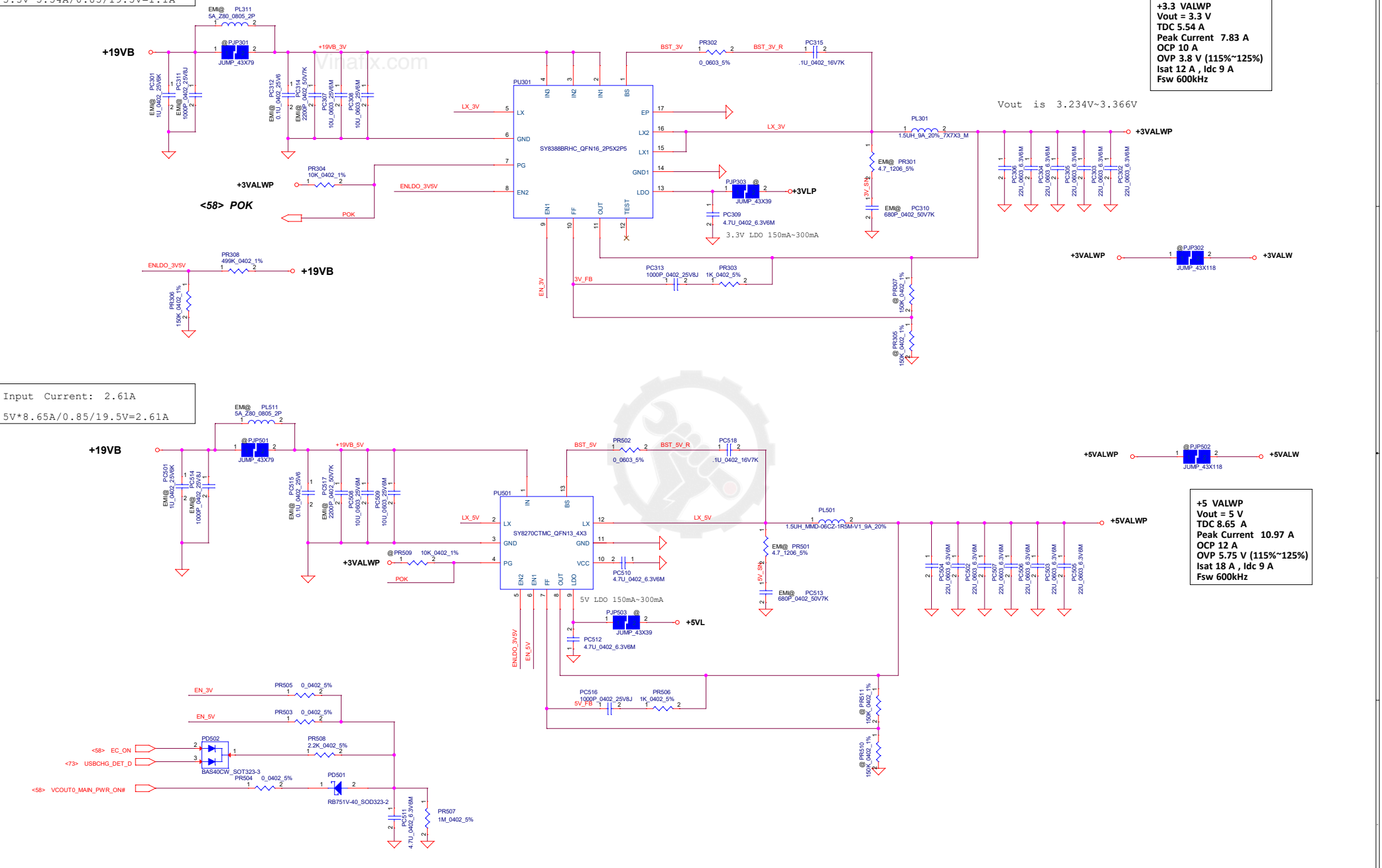


Input Current: 1.1A  
 $3.3V \times 5.54A / 0.85 / 19.5V = 1.1A$

**+3.3 VALWP**  
Vout = 3.3 V  
TDC 5.54 A  
Peak Current 7.83 A  
OCP 10 A  
OVP 3.8 V (115%~125%)  
Isat 12 A, Idc 9 A  
Fsw 600kHz

Input Current: 2.61A  
 $5V \times 8.65A / 0.85 / 19.5V = 2.61A$

**+5 VALWP**  
Vout = 5 V  
TDC 8.65 A  
Peak Current 10.97 A  
OCP 12 A  
OVP 5.75 V (115%~125%)  
Isat 18 A, Idc 9 A  
Fsw 600kHz

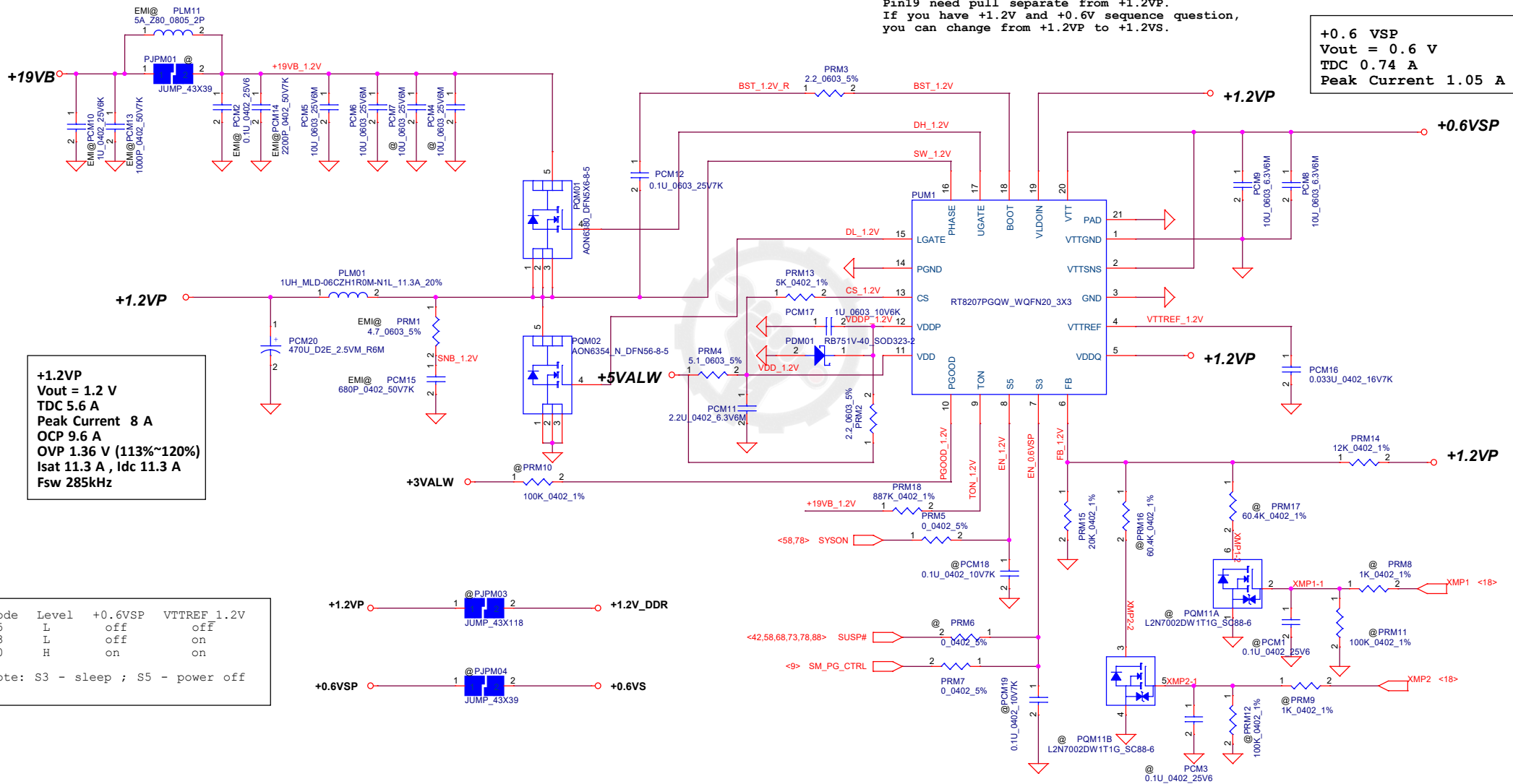




$$1.2V \cdot 5.6A / 0.85 / 19.5V = 0.41A$$

Pin19 need pull separate from +1.2VP.  
If you have +1.2V and +0.6V sequence question,  
you can change from +1.2VP to +1.2VS.

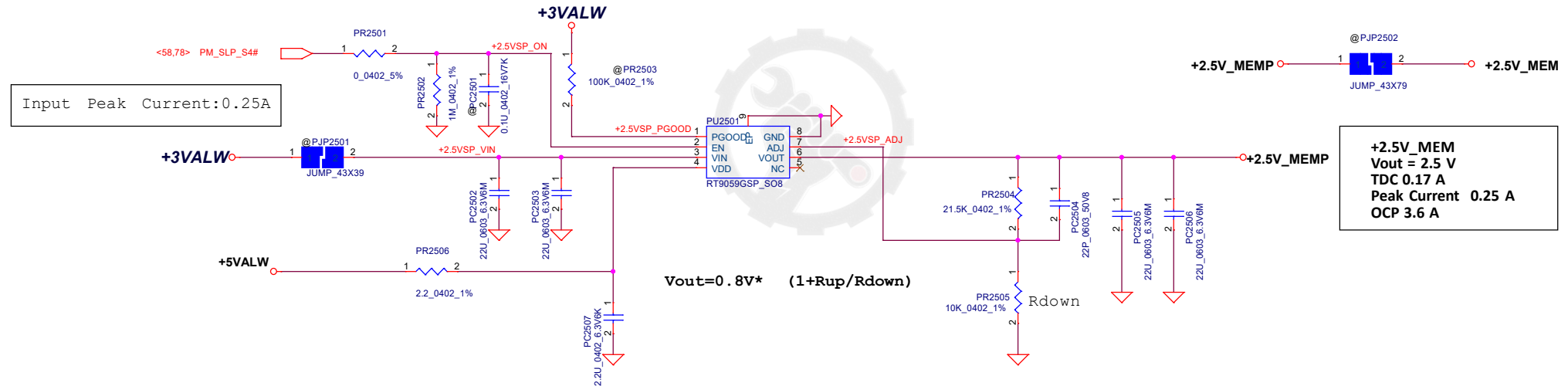
```
+0.6 VSP
Vout = 0.6 V
TDC 0.74 A
Peak Current 1.05 A
```



Mode	Level	+0.6VSP	VTTREF 1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

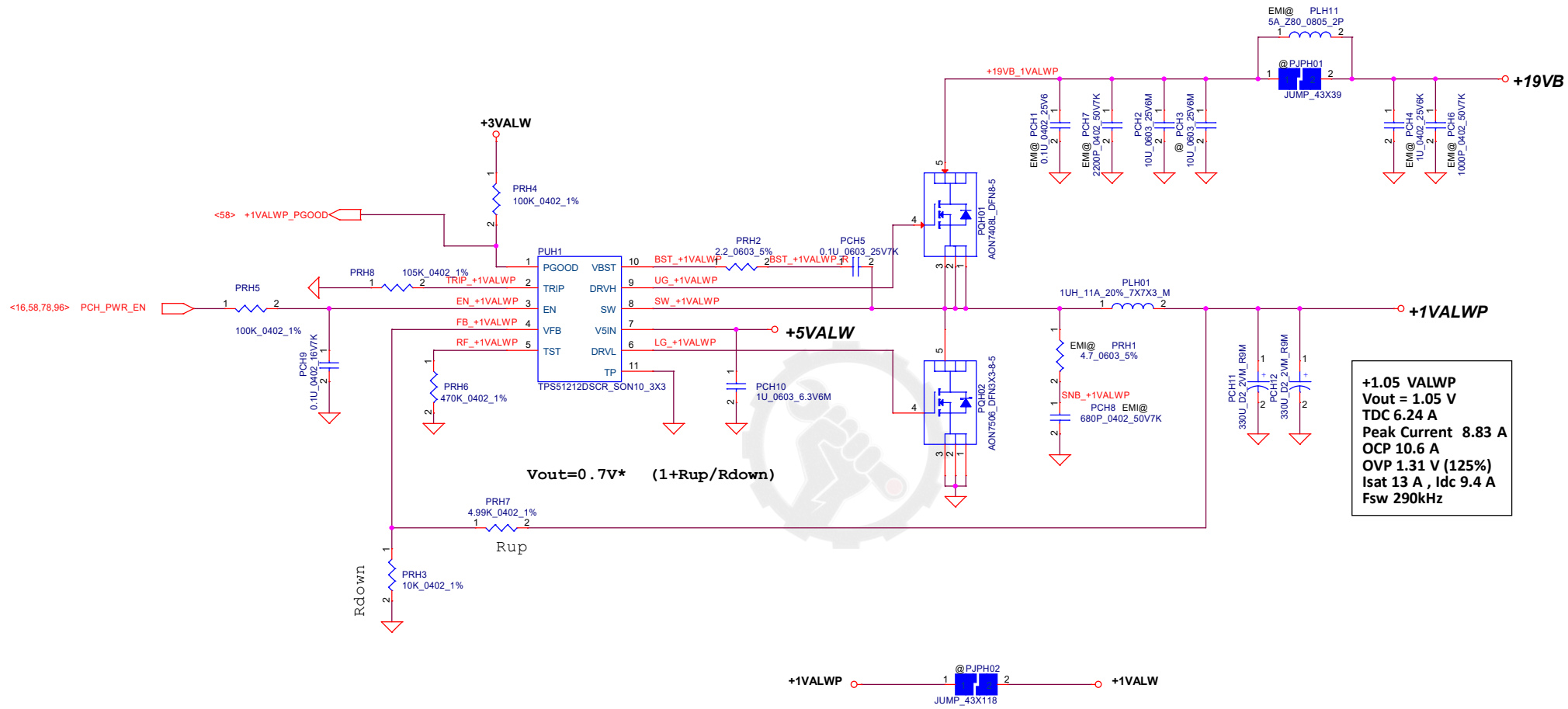
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title			
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				Size	Document Number	Rev	
				LA-G881P0.1			
Date:				Thursday, May 30, 2019		Sheet	85 of 109



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Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title	
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					LA-G881P
				Date	Thursday, May 30, 2019
				Sheet	86 of 109
				Rev	0.1

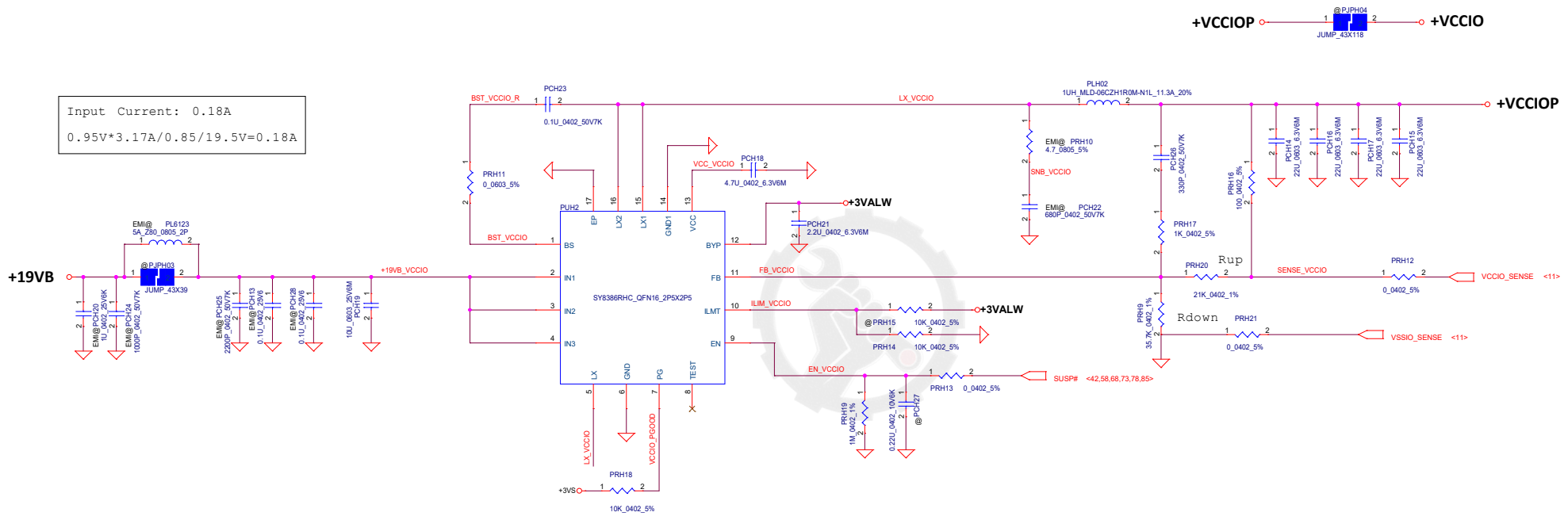
Vinafix.com

Input Current: 0.4A  
 $1.05V \times 6.24A / 0.85 / 19.5V = 0.4A$

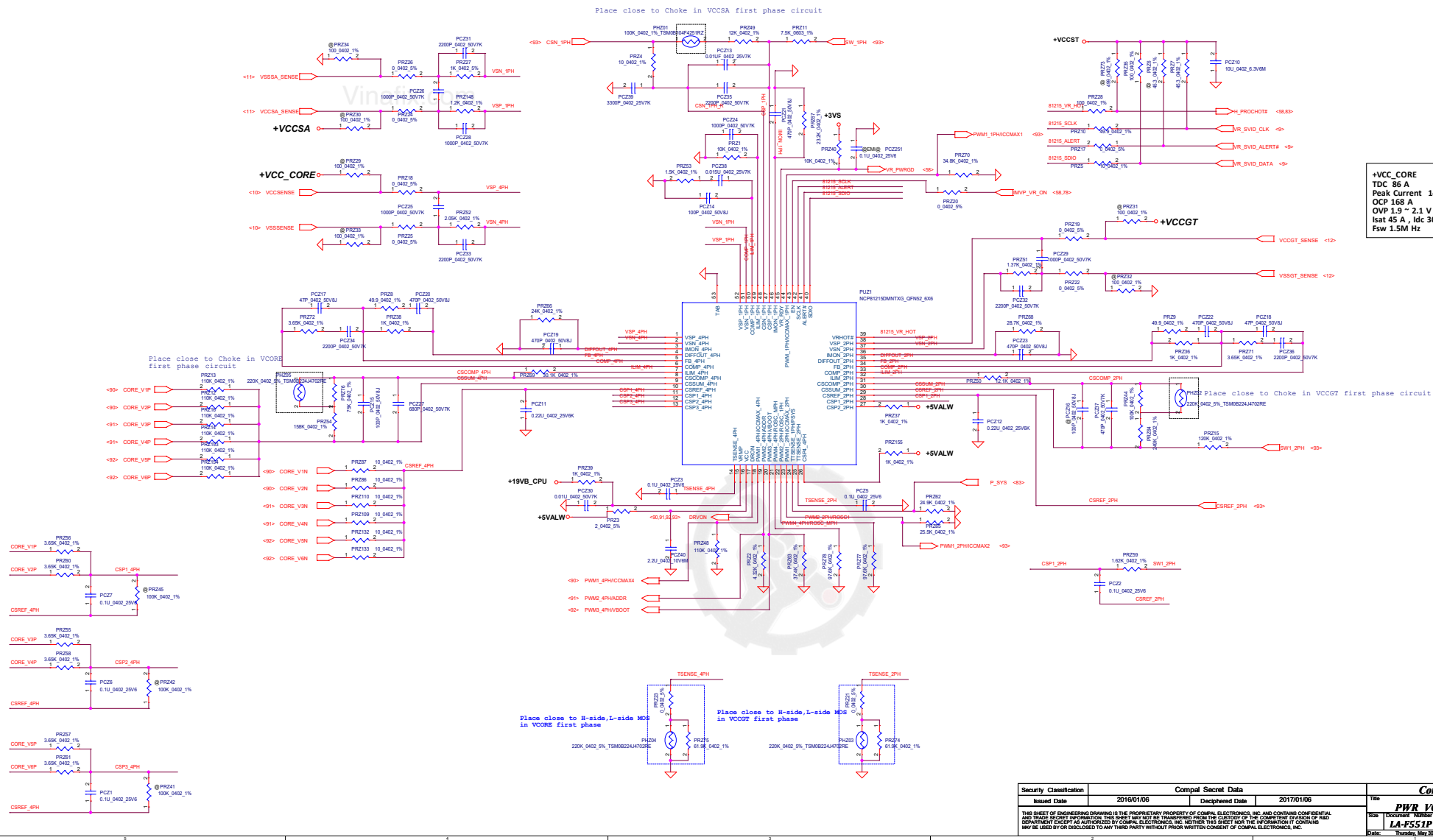


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title	
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Size		Document Number			Rev
		LA-G881P			0.1
Date:		Thursday, May 30, 2019		Sheet	87 of 109

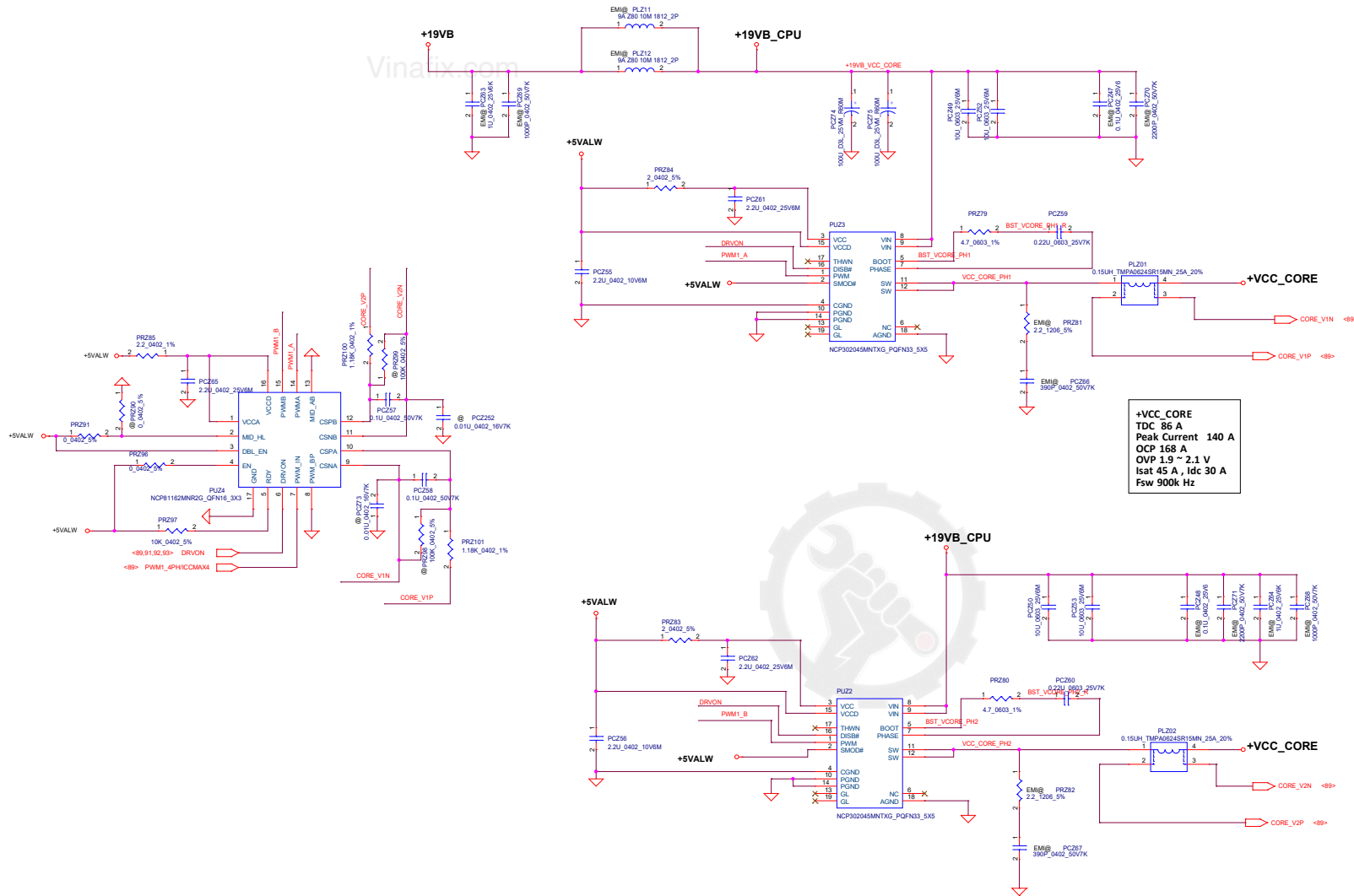
+VCCIOP (0.95V)  
Vout = 0.95 V  
TDC 3.17 A  
Peak Current 4.48 A  
OCP 6 A  
OVP 1.14 V (120%)  
Isat 11.3 A , Idc 11.3 A  
Fsw 500kHz

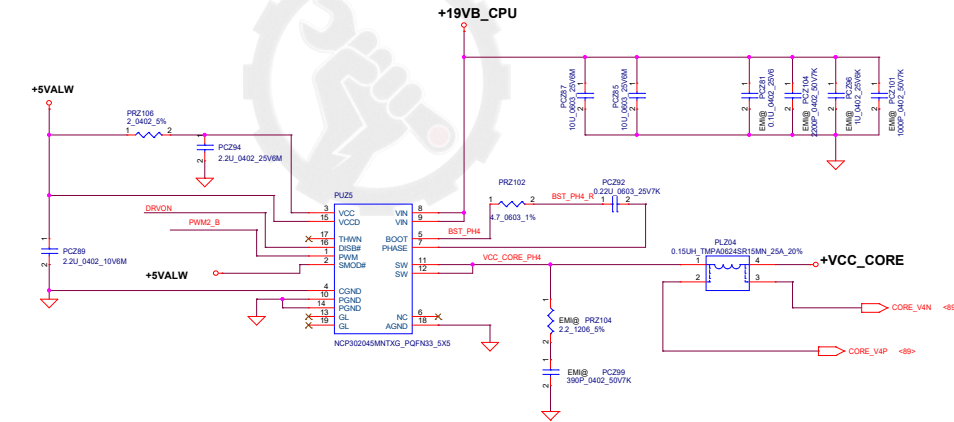
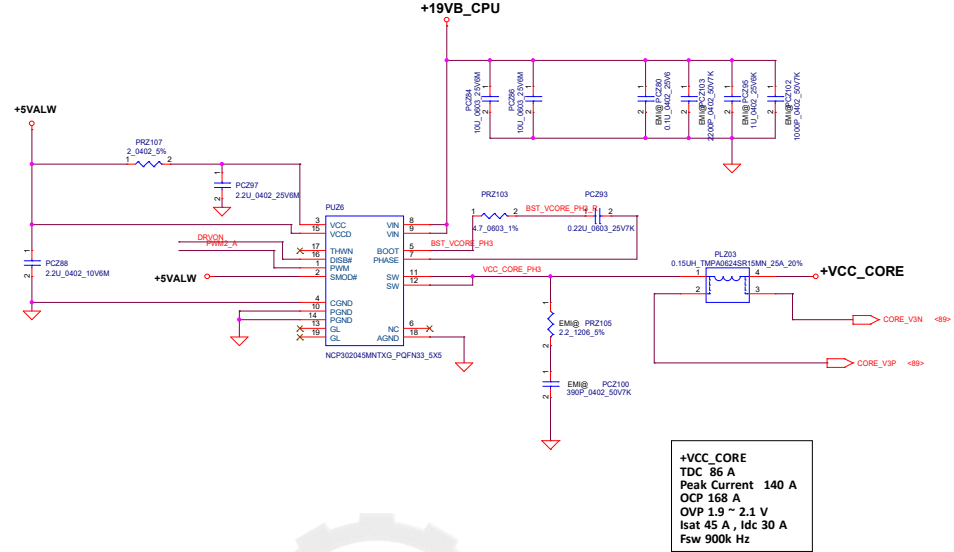
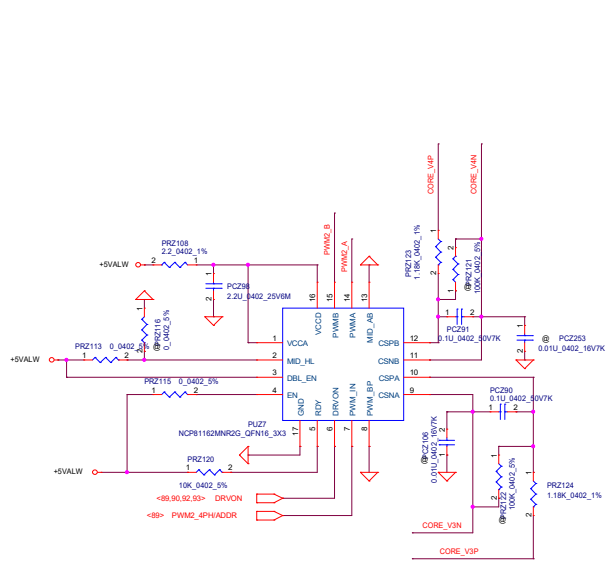


Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title	<b>PWR +VCCIO</b>	
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					<b>LA-G881P</b>	0.1
				Date:	Thursday, May 30, 2019	Sheet 88 of 109



Security Classification	Compul Secret Data		Title	
Issued Date	2016/01/06	Decpched Date	2017/01/06	PWR VCore NCP82125 LA-551P
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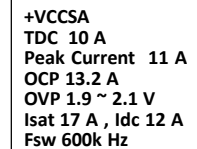
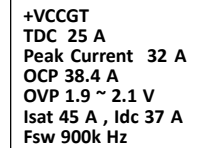


+VCC\_CORE  
TDC 86 A  
Peak Current 140 A  
OCP 168 A  
OVP 1.9 ~ 2.1 V  
Isat 45 A, Idc 30 A  
Fsw 900k Hz





## +19VB\_CPU



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+VCC\_CORE

+VCC CORE

470uF\_D2 x2  
47uF\_0805 X 4  
47uF\_0603 X 4  
22uF\_0603 X 20  
10uF\_0402 X 10  
1uF\_0201 X 48

+VCCGT

+VCCGT

470uF\_D2 x1  
47uF\_0805 X 11

+VCCSA

+VCCSA

47uF\_0603 X 4  
22uF\_0603 X 6

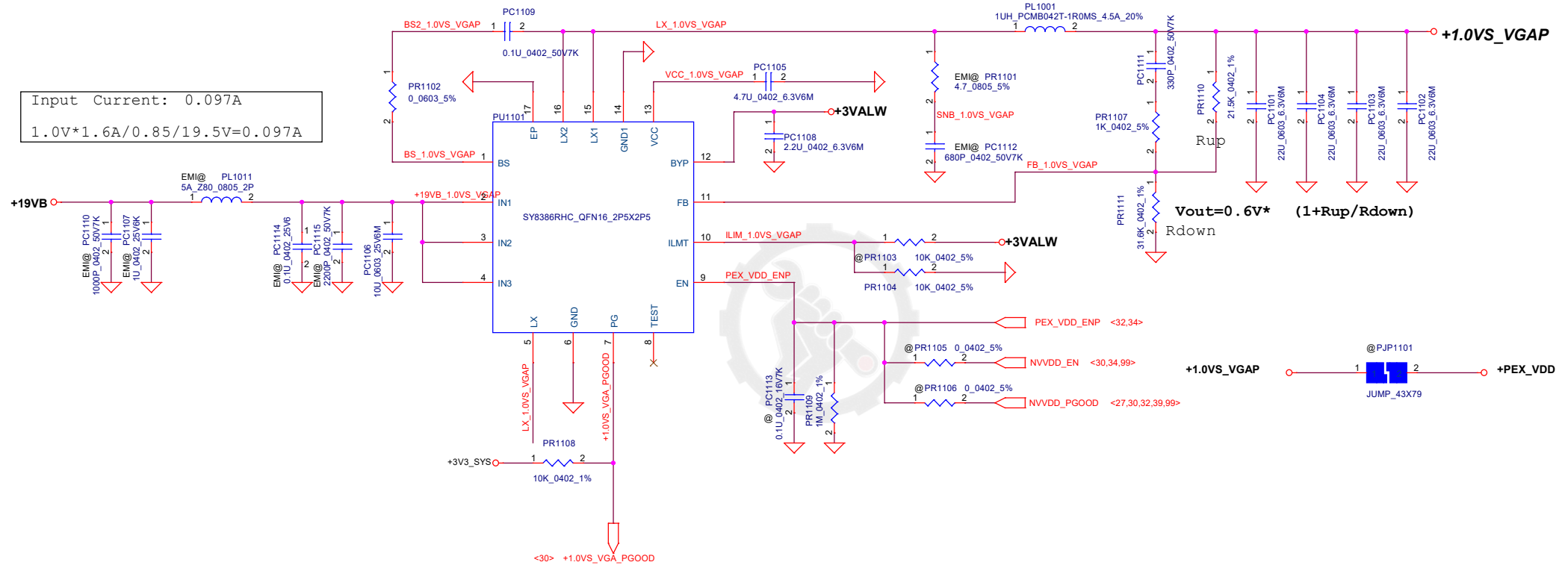


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Issued Date	2018/05/16	Deciphered Date	2018/12/31	Title	PWR CPU DECOUPLING
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Input Current: 0.097A

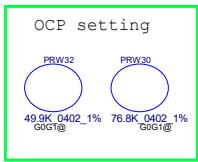
$1.0V \cdot 1.6A / 0.85 / 19.5V = 0.097A$

+1.0VS VS\_VGAP  
Vout = 1.0 V  
TDC 1.6 A  
Peak Current 2.26 A  
OCP 6 A  
OVP 1.2 V (120%)  
Isat 7 A , Idc 4.5 A  
Fsw 500kHz



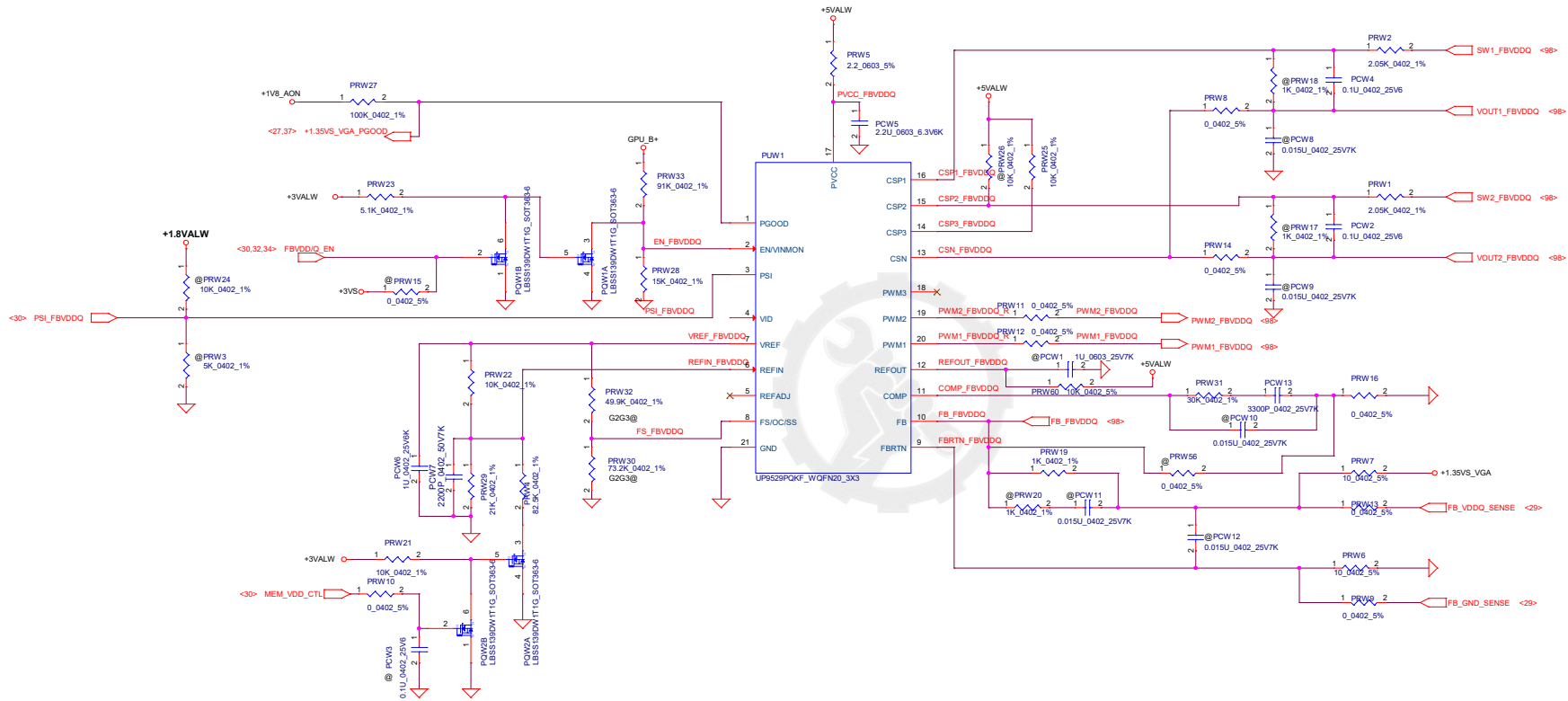
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR +1.0VS VGAP</b>	
Issued Date	2018/08/07	Deciphered Date	2019/08/07		
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				Size	Document Number
				<b>LS-G88BP</b>	
Date: Thursday, May 30, 2019				Sheet	95 of 109





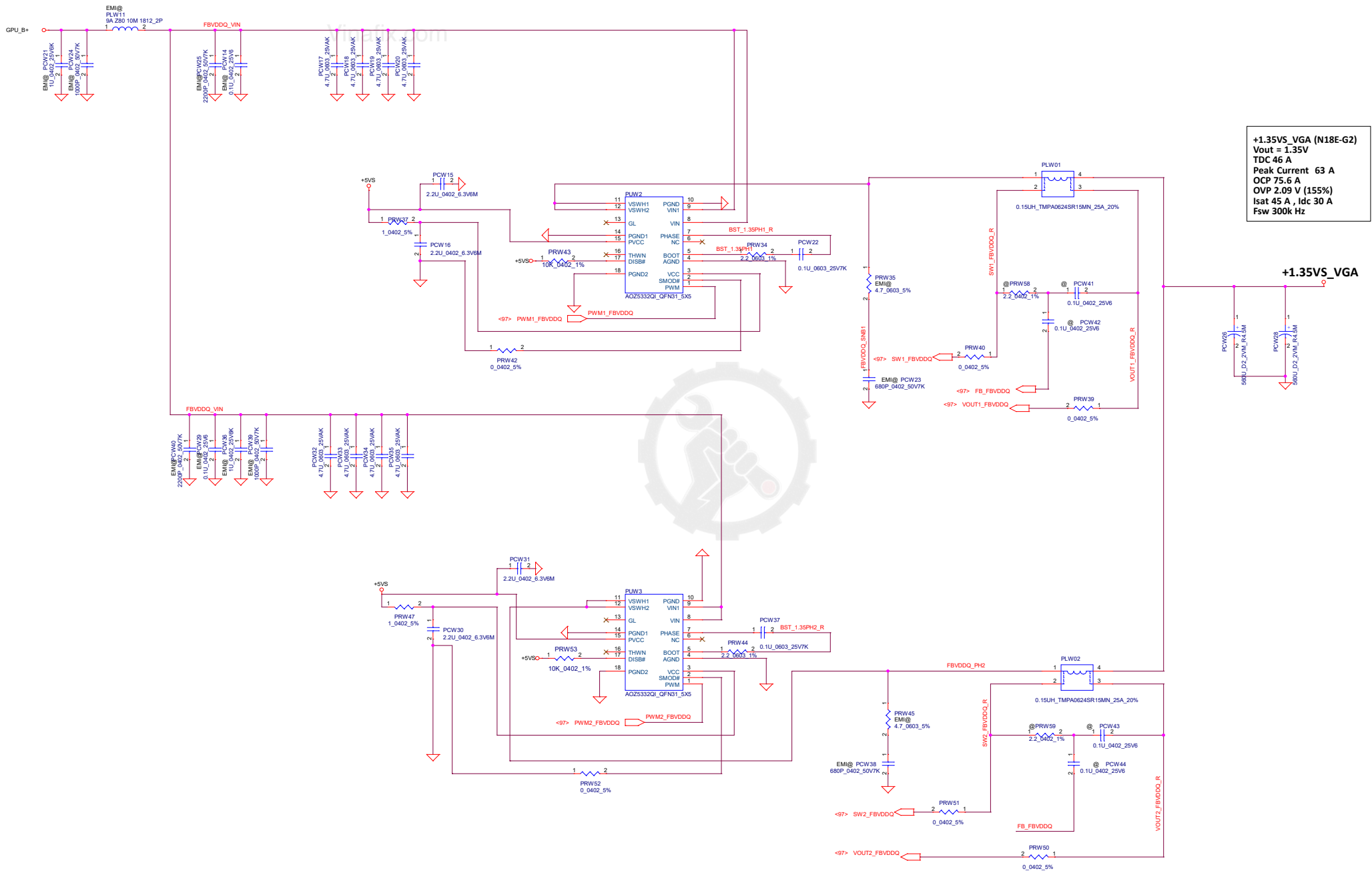
Vinafix.com

+1.35VS\_VGA (N18E-G2)  
Vout = 1.35V  
TDC 46 A  
Peak Current 63 A  
OCP 75.6 A  
OVP 2.09 V (155%)  
Isat 45 A, Idc 30 A  
Fsw 300kHz



BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW26	PRW27
	N18E G2/G3			1.25V & 1.35V	21K	82.5K

Security Classification		Compal Secret Data		Title	
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Size	Document Number
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Date: Thursday, Mar 30, 2019				Sheet	97 of 109



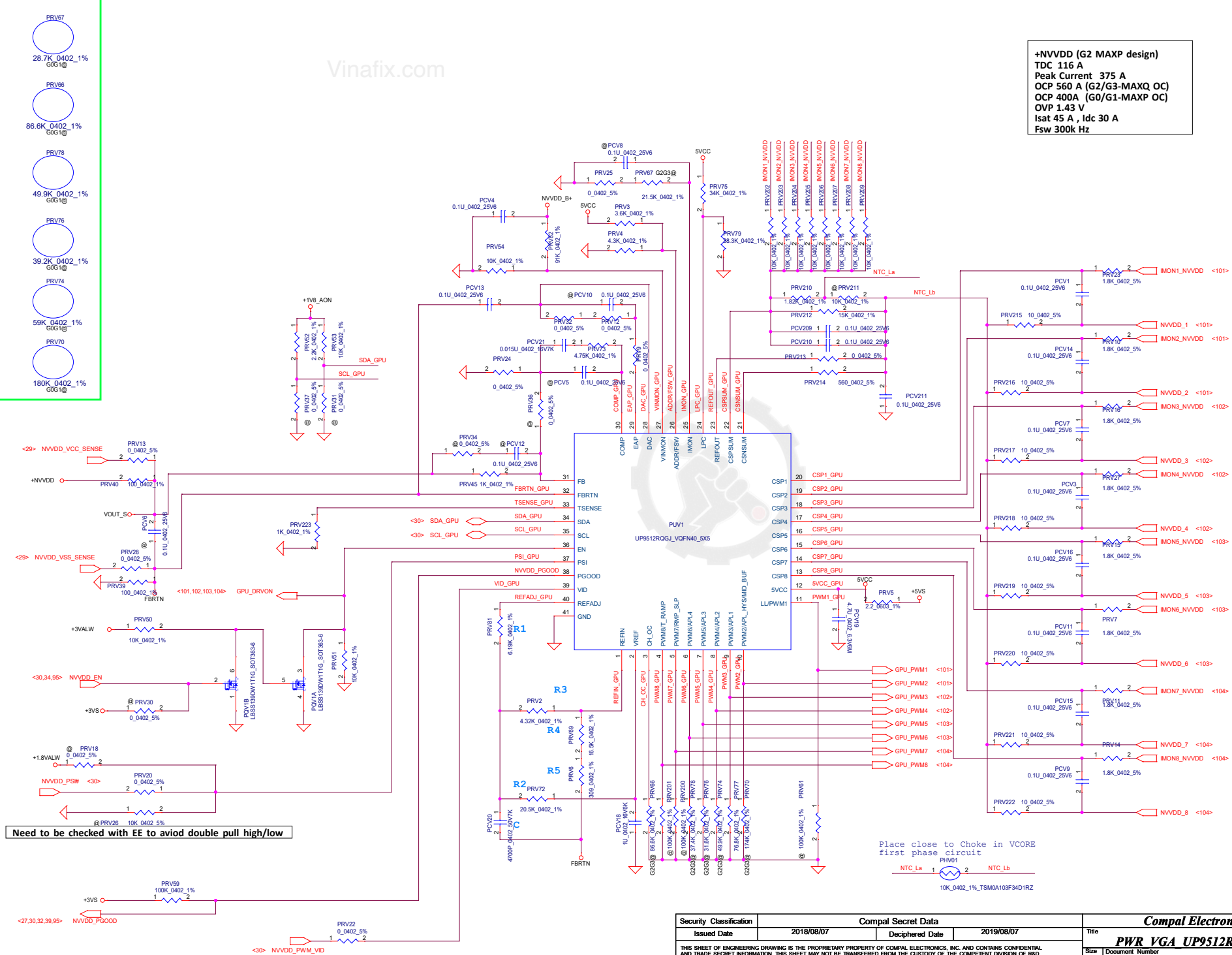
**+1.35VS\_VGA (N18E-G2)**  
Vout = 1.35V  
TDC 46 A  
Peak Current 63 A  
OCP 75.6 A  
OVP 2.09 V (155%)  
Isat 45 A, Idc 30 A  
Fsw 300k Hz

**+1.35VS\_VGA**

OCP setting

Vinafix.com

+NVVDD (G2 MAXP design)  
TDC 116 A  
Peak Current 375 A  
OCP 560 A (G2/G3-MAXQ OC)  
OCP 400A (G0/G1-MAXP OC)  
OVP 1.43 V  
Isat 45 A, Idc 30 A  
Fsw 300k Hz



Need to be checked with EE to avoid double pull high/low

Place close to Choke in VCORE first phase circuit

NTC\_La 10K\_0402\_1% TSM0103F34D1R2

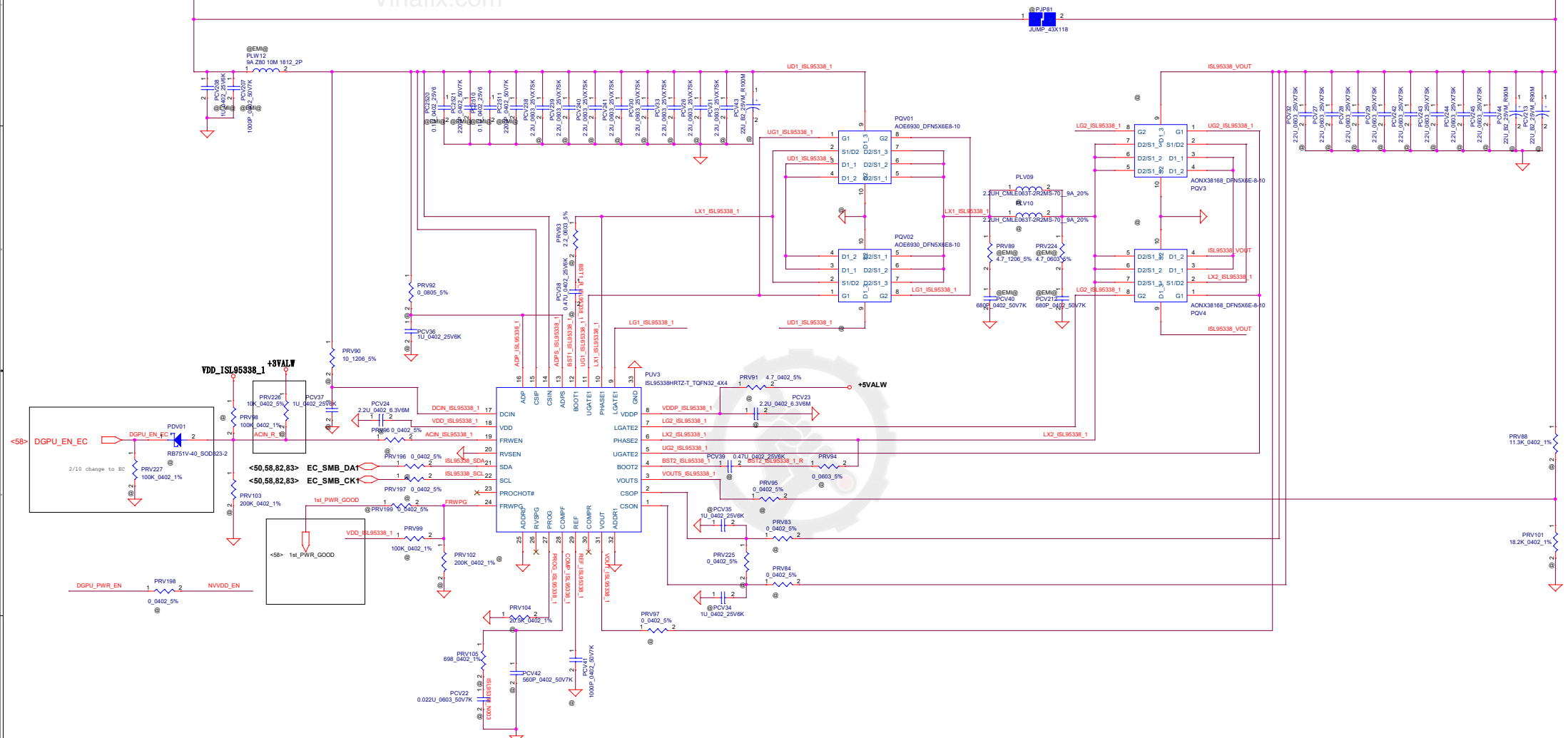
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2018/08/07	Deciphered Date	2019/08/07	Title	PWR VGA UP9512R
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Input Current : 7.24 A

15A\*8V/0.85/19.5V=7.24A

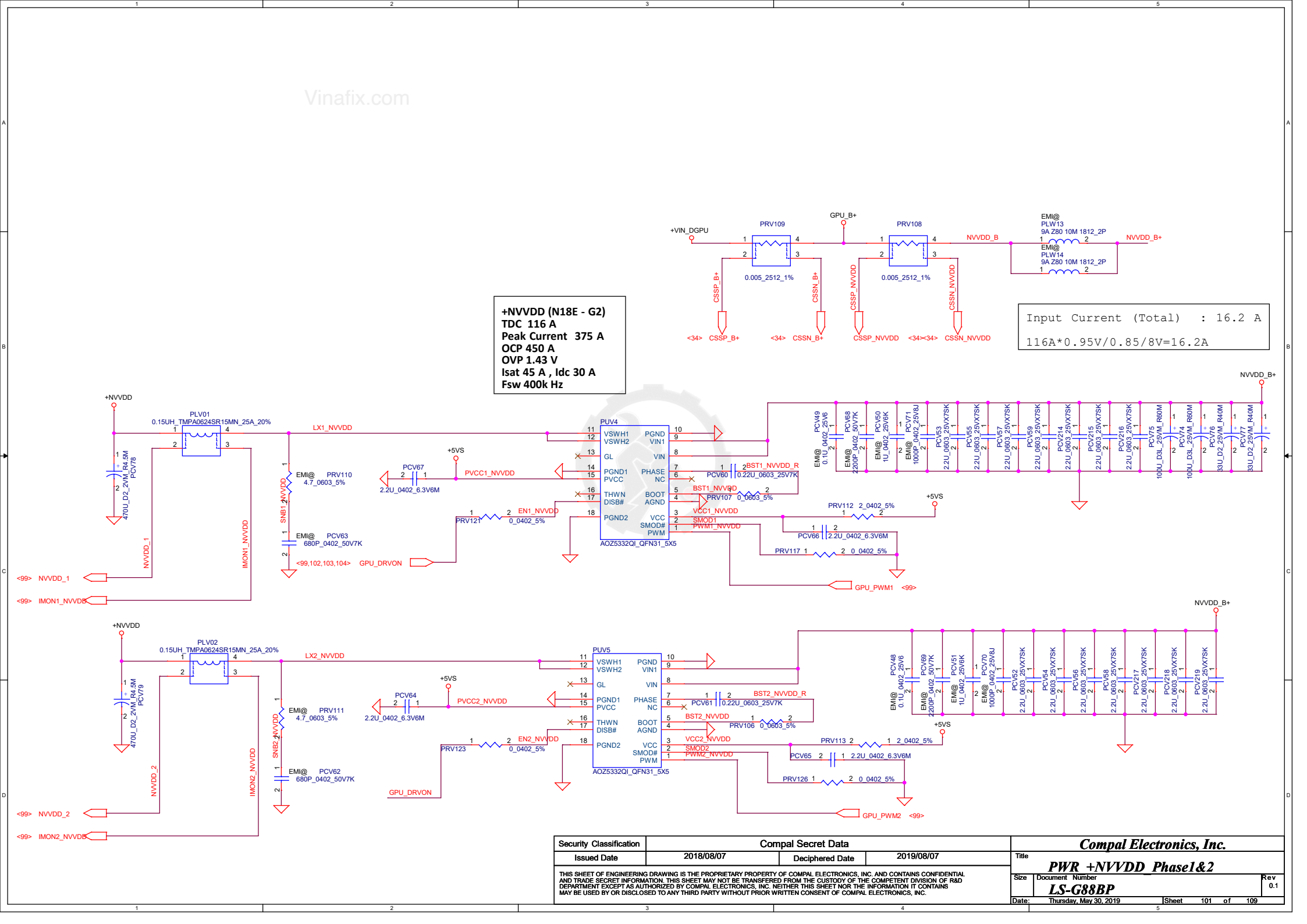
+VIN\_DGPU (N18E - G2)  
Vout = 8V  
TDC 15 A  
OCP = 30 A  
Isat 37 A, Idc 30 A  
Fsw = 620k Hz

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				PWR 1st Stage(ISL95338)	
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**+NVVDD (N18E - G2)**  
**TDC 116 A**  
**Peak Current 375 A**  
**OCP 450 A**  
**OVP 1.43 V**  
**Isat 45 A , Idc 30 A**  
**Fsw 400k Hz**

Input Current (Total) : 16.2 A  
 $116A \cdot 0.95V / 0.85 / 8V = 16.2A$

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**+NVVDD (N18E - G2)**  
TDC 116 A  
Peak Current 375 A  
OCP 450 A  
OVP 1.43 V  
Isat 45 A , Idc 30 A  
Fsw 400k Hz

Input Current (Total) : 16.2 A  
 $116A \cdot 0.95V / 0.85 / 8V = 16.2A$

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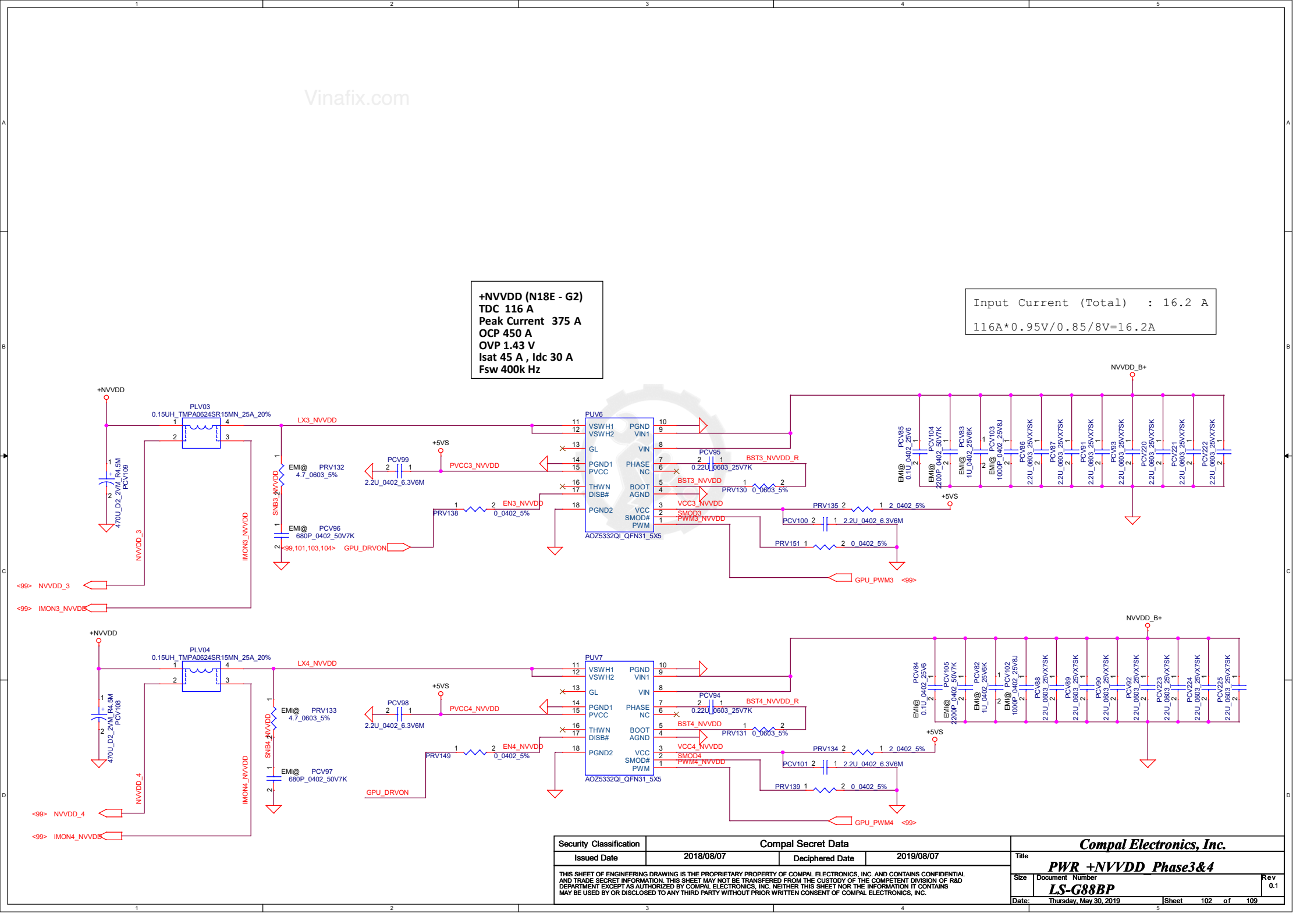
**+NVVDD (N18E - G2)**  
TDC 116 A  
Peak Current 375 A  
OCP 450 A  
OVP 1.43 V  
Isat 45 A , Idc 30 A  
Fsw 400k Hz

Input Current (Total) : 16.2 A  
 $116A \cdot 0.95V / 0.85 / 8V = 16.2A$

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**+NVVDD (N18E - G2)**  
TDC 116 A  
Peak Current 375 A  
OCP 450 A  
OVP 1.43 V  
Isat 45 A , Idc 30 A  
Fsw 400k Hz

Input Current (Total) : 16.2 A  
 $116A \cdot 0.95V / 0.85 / 8V = 16.2A$

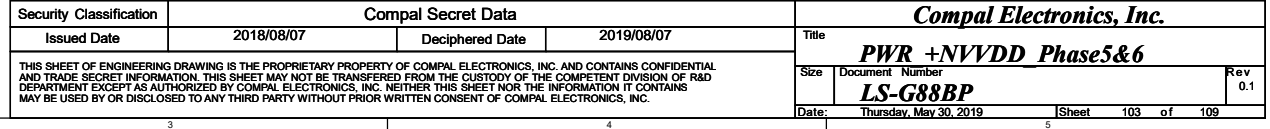


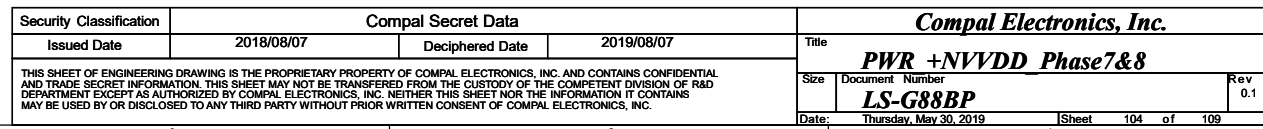
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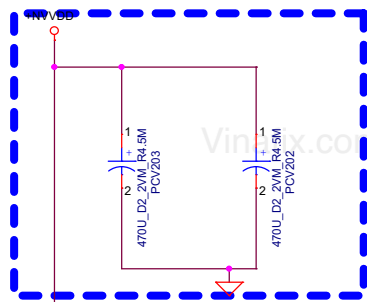
**+NVVDD (N18E - G2)**  
TDC 116 A  
Peak Current 375 A  
OCP 450 A  
OVP 1.43 V  
Isat 45 A , Idc 30 A  
Fsw 400k Hz

Input Current (Total) : 16.2 A  
 $116A \cdot 0.95V / 0.85 / 8V = 16.2A$

Input Current (Total) : 16.2 A
$116\text{A} \times 0.95\text{V} / 0.85 / 8\text{V} = 16.2\text{A}$



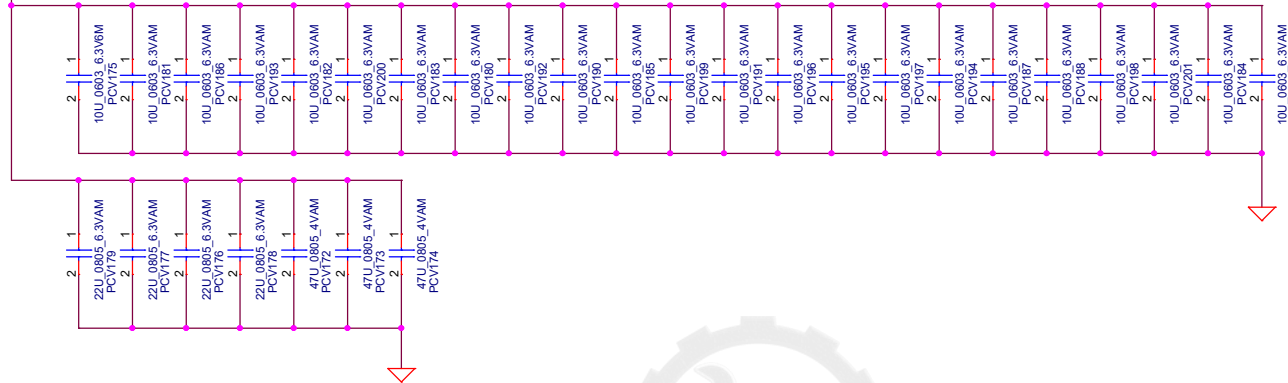




Place near GPU

+NVVDD			
470uF	D2	X	2
47uF	0805	X	3
22uF	0805	X	4
10uF	0603X		23

Place under GPU

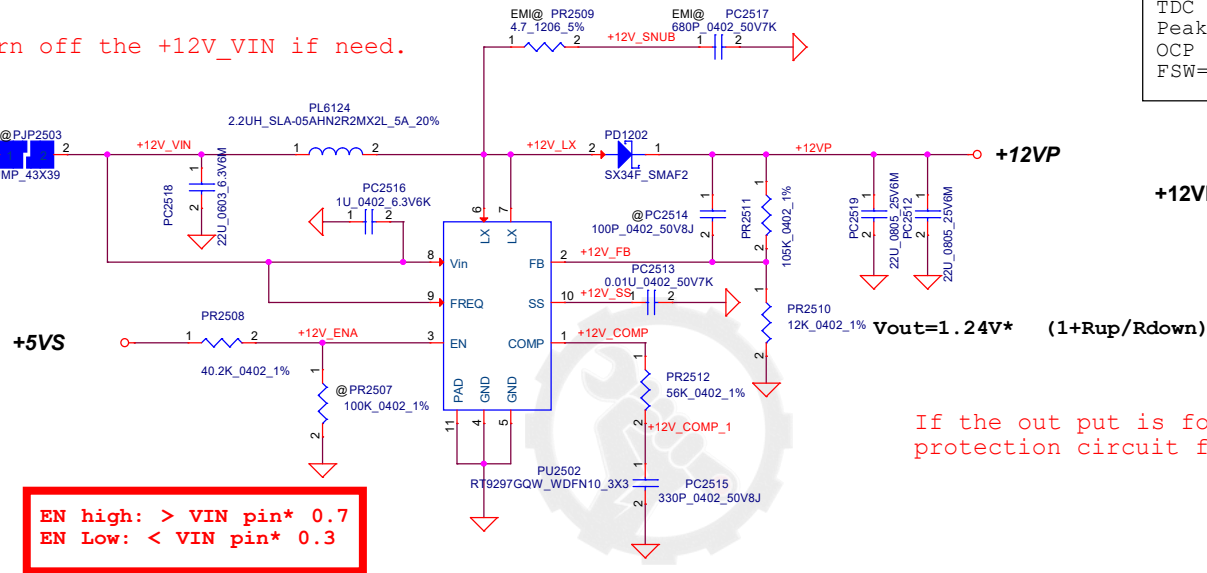


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Add a switch circuit to turn off the +12V\_VIN if need.

Input Current: 1.58A  
 $12V \times 0.56A / 0.85 / 5V = 1.58A$

+12VP  
 Vout = 12 V  
 TDC 0.56A  
 Peak Current 0.8 A  
 OCP current 3A  
 FSW=1.24MHz



If the out put is for I/O port, should be add protection circuit for I/O short protection.

+12VP  
 +12V\_FAN

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1	P. 68 P. 69 P. 70 P. 72	PWR_VDDC_NCP81022 PWR_VDDC-Phase1&2 PWR_VDDC-Phase3&4 PWR_VDDCI	2017/08/14	Compal_PWR	1.AMD schematic error : CPU "DRVON" and GPU "DRVON" use the same net name.	1.Change net name from "DRVON" to "DRVON_GPU".	0.1
2	P.67	PWR +1.8VSP/ +1.8VSP_AUDIO	2017/08/15	Compal_HW	1.1.8VSP enable signal's sequence have wrong. Cause to PM_SLF_S5# pull low.	1.Change 1.8VSP enable signal change from SUSP# to PCH_PWR_EN. 2.Add enable signal pull high 10K ohm to +3VALW 3.PR807/PR808 un-pop.	0.1
3	P.67	PWR +1.8VSP/ +1.8VSP_AUDIO	2017/08/15	Compal_HW	1.Need another 1.8V supply to audio codec and usb retimer.	1.Add RT9013 LDO Circuit.	0.1
4	P.66	PWR_+1VALWP	2017/08/15	Compal_HW	1.Modify enable signal RC delay.	1.Change PR300 from 0 ohm to 100K ohm. 2.PC300 0.1uF pop.	0.1
5	P.75	PWR_VCORE_NCP81215	2017/08/17	Compal_PWR	1.PWR and HW side double pull high/down.	1.PR500,PR514,PR521,PR526,PR528,PR531 un-pop.	0.1
6	P.75	PWR_VCORE_NCP81215	2017/08/22	Compal_PWR	1.Modify ICCMAX=150A and OCP=180A.	1.Change PR558 from 100K ohm to 118K ohm. 2.Change PR541 from 27.4K ohm to 32.4K ohm.	0.1
7	P.67	PWR +VGA_PCIE/ +1.8VGSF	2017/09/04	Compal_PWR	1.Because Choke material will be EOL,we change choke source to substitute material.	1.Change PR800 from SH00000TV00 to SH000019300.	0.1A
8	P.71	PWR +1.8VSP/ +1.8VSP_AUDIO	2017/09/04	Compal_HW	1.Modify 1.8VSP enable signal and RC delay time.	1.Delete PR817. 2.Add PR807 100K ohm. 3.Add PC811 0.1uF. 4.Add PR808 1M ohm.	0.1A
9	P.68/70	PWR_VDDC_NCP81022/ PWR_VDDC-Phase3&4	2017/09/04	Compal_PWR	1.Because VGA Chip type change from 560 to 570,we need to change 3+1 phase to 4+1 phase.	1.Add PU6301,PL6300,PR6309,PR6310,PR6311,PC6305,PC6306,PC6307,PC6308,PC6309,PC6310,PC6311,PC6312,PC6313,PC6314,PC6315,PC6316,PR6026,PR6029,PR6044. 2.Change PR6016 from 82.5K ohm to 19.6K ohm. 3.Change PR6047 from 22.1K ohm to 45.3K ohm. 4.Delete PR6085,PR6086.	0.1A
10	P.76/77	PWR_VCORE_VCC_CORE/ +VCC_GT	2017/09/11	Compal_ME	1.CPU choke's height are difference with Cassini. VCORE and VCCGT 's choke height change from 3mm to 4mm.	1.Change PL501,PL502,PL503,PL505,PL506 from SH00001DC00 to SH00001EE00.	0.2
11	P.67	PWR +VGA_PCIE/ +1.8VGSF	2017/09/11	Compal_PWR	1.Choke substitute material change to main source.	1.Change PL800 from SH0000019300 to SH00000TV00.	0.2
13	P.71/68	PWR +1.8VSP/ PWR_VDDC_NCP81022	2017/09/13	Compal_HW	1.Modify 1.8VS net name.	1.Net name +1.8VS change to +1.8VALW.	0.2
14	P.73	PWR_+1.5V_VGA	2017/09/13	Compal_PW	1.Modify OCP resistor.	1.Change PR8206 from 8.66K ohm to 6.81K ohm.	0.2
15	P.61	DCIN / BATT CONN / OTP	2017/09/14	Compal_PW	1.Unify mos materials.	1.Change PQ9 from SB00000ZU00 to SB00000PV00.	0.2

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9	P.75	PWR_VCORE_NCP81215	2017/09/14	Compal_PWR	1.Change Output Choke DCR from 0.9mohm to 0.67mohm (+/-5%).Fine tune FB sense and CSCOMP RC value.	1.Change PR546,PR550,PR551,PR572 from 115K to 90.9K ohm. 2.Change PR557,PR587,PR581,PR582,PR595 from 1.62K to 2.21K ohm. 3.Change PR538 from 25.5K to 28.7K ohm. 4.Change PR549 from 100K to 90.9K ohm. 5.Change PC528 from 560pF to 680pF. 6.PC505,PC523 un-pop. 7.Change PC525,PC527 from 0.1uF to 0.22uF. 8.Change PR527 from 1Kohm to 1.37Kohm. 9.Change PR511 from 1.65Kohm to 1.58Kohm. 10.Change PR512 from 31.6Kohm to 28.7Kohm. 11.Change PC509 from 10nF to 15nF. 12.Change PC510 from 56pF to 100pF. 13.Change PR548 from 261Kohm to 249Kohm.	0.2
10	P.61	DCIN / BATT CONN / OTP	2017/09/26	Compal_EMI	1.EMI request to modify VIN beed.	1.Change PL1,PL3 from SM01000P500 to SM01000DJ00. 2.Change PC2,PC4 from 100pF to 1000pF.	0.2
11	P.68	PWR_+VDDC_NCP81022	2017/12/14	Compal_HW	1.HW request to change NCP81022 PWROK signal.	1.PR6008 unpop. 2.Add PR6091 0 ohm 0402. 2.Add Signal VGA_PWROK to pin1 PWROK.	0.3
12	P.75	PWR_VCORE_NCP81215	2017/12/14	Compal_PWR	1.NCP81215 change PA0 version P/N.	1.Change PU500 from SA0000AQE00 to SA0000BNK10.	0.3
13	P.61	PWR DCIN / BATT CONN / OTP	2017/12/14	Compal_PWR	1.Main source SB00000Z500 EOL.	1.Change PQ2 from SB00000Z500 to SB000002R00.	0.3
14	P.76/77	PWR_VCORE_+VCC_CORE	2017/12/14	Compal_PWR	1.Cytec choke SH00001DA00 VRTT fail 2.SA choke change common part include SH000015M00 & SH000015P00.	1.Change PL501,PL502,PL503,PL505,PL506 from SH00001EE00 to SH00001D800. 2.Change PL508 from SH000015M00 to SH00001ED00.	0.3
15	P.64/66/73	PWR_+1.2VP/+0.6VSP PWR_+1VALWP PWR_+1.5V_VGAP	2017/12/14	Compal_PWR	1.Because of polyma cap non equal substitue, all 220uF H=1.9 polyma cap are unified SGA00009800.	1.Change PC209,PC215,PC306,PC307,PC8207,PC8208 from SGA20221D40 to SGA00009800.	0.3
16	P.68	PWR_+VDDC_NCP81022	2017/12/14	Compal_PWR	1.Unify all 100K_0402 thermistor as SL20002H00.	1.Change PH6000,PH6001 from SL200000U00 to SL200002H00.	0.3
17	P.68	PWR_+VDDC_NCP81022	2017/12/14	Compal_PCE	1.PCE team request to change for cost reduction action.	1.Change PC6007,PC6019 from SE00000FD80(330pF_0402_25V) to SE000006I80(330pF_0402_50V).	0.3
18	P.75	PWR_VCORE_NCP81215	2017/12/14	Compal_PWR	1.VRTT test for IA & GT main and 2nd Choke to fine tune IMON resistor.	1.Change PR534 from 24.9K to 26.7K. 2.Change PR538 from 28.7K to 30.9K.	0.3
19	P.73	PWR_+1.55VRAM	2017/12/14	Compal_PWR	1.Modify OCP resistor setting for main/2nd mos.	1.Change PR8206 from 6.81K to 7.15K.	0.3
20	P.72/73	PWR_+NVDD2 PWR_+1.55VRAM	2017/12/14	Compal_PWR	1.Because thermal derating fail,we change capcitor type.	1.Change PC710,PC8200 from SE000006S80 to SE00000GC00.	0.3
21	P.68	PWR_+VDDC_NCP81022	2017/12/26	Compal_HW	1.Modify pull high/low resistors on the SVI2 interface.	1.Change PR6001 from 1K to 10K. 2.Change PR6006 from 1K to 10K.	0.3
22	P.69/70/72	PWR_+VDDC-Phase1&2 PWR_+VDDC-Phase3&4 PWR_+VDDCI	2017/12/27	Compal_PWR	1.Because SE000003H00 sample dilevery is poor,we change capcitor from X5R to X7R.	1.Change PC6118,PC6206,PC6218,PC6306,PC6401 from SE000003H00 to SE00000GC00.	0.3

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